

**CPU CORE**  
SENTTECH  
SC451  
Page: 25

**+3VPCU  
+3V\_S5/+3VSUS  
+3V  
+5VSUS/+5V  
10V/15V  
+1.8V\_S5**  
MAXIM  
MAX8744ETJ+  
Page: 26

**+1.8VSUS/+1.8V  
+1.2V**  
MAXIM  
MAX8743EEI  
Page: 27

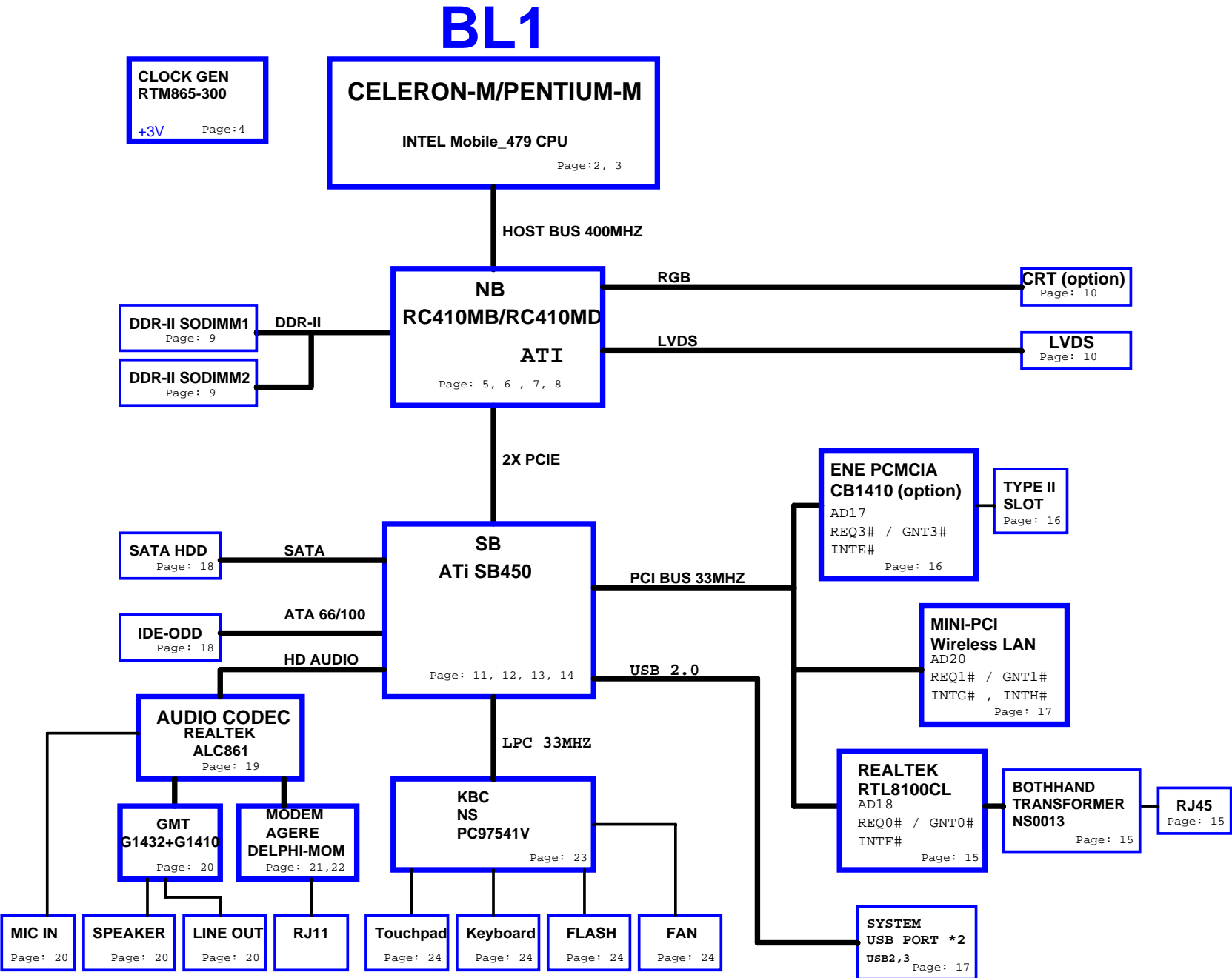
**+1.05V**  
SENTTECH  
SC4215\*2  
Page: 29

**+0.9VSUS  
+0.9V**  
GMT  
G2996  
Page: 26, 29

**BATTERY CHARGER**  
MAXIM  
MAX8724  
Page: 28

**Power State Table**

Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+5VPCU	N/A	ALWAYS	VIN
+5V_S5	S5_ON	S0-S5	+5VPCU
+5VSUS	SUSON	S0-S3	+5VPCU
+5V	MAINON	S0	+5VPCU
15V/10V	N/A	S0	+5VPCU
+1.2V	MAINON	S0	VIN
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS

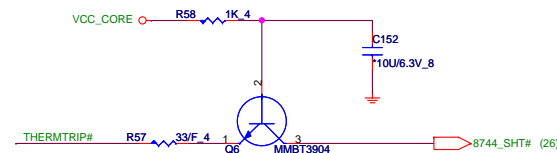
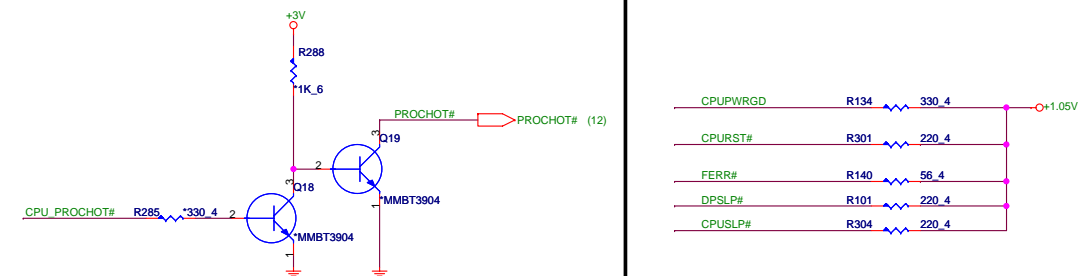




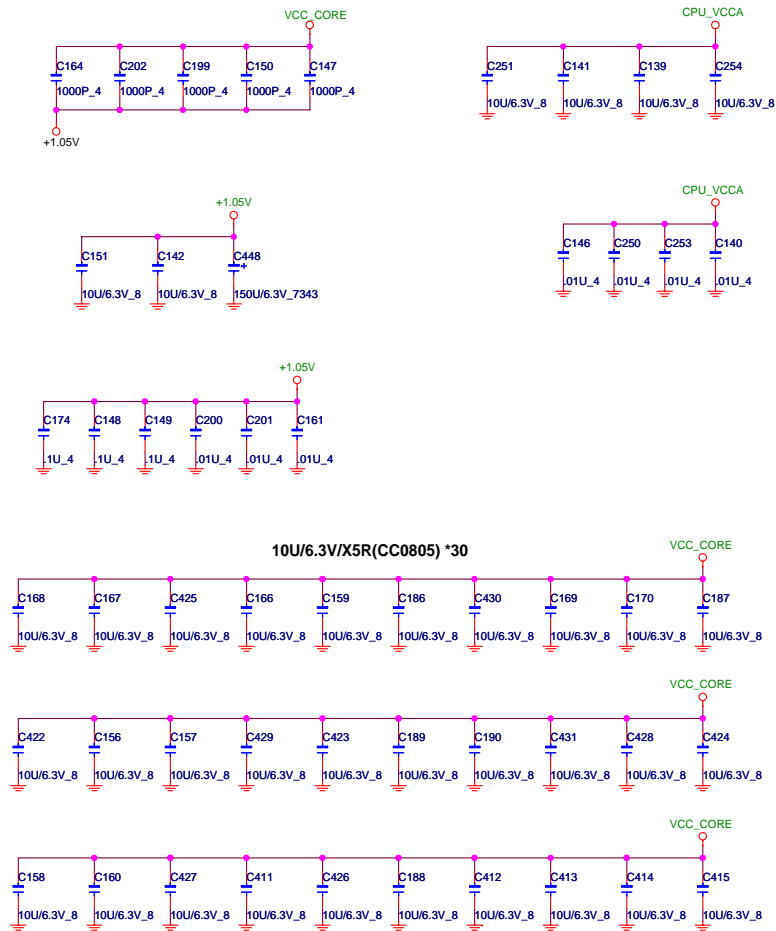
SMB setting : thermal Alert temp is 85  
thermal over temp is 127



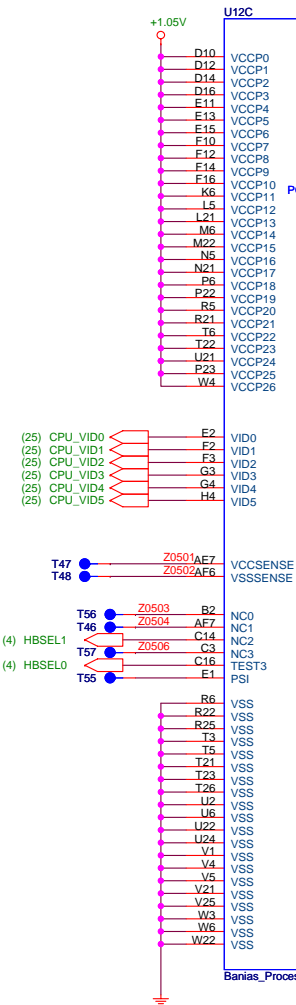
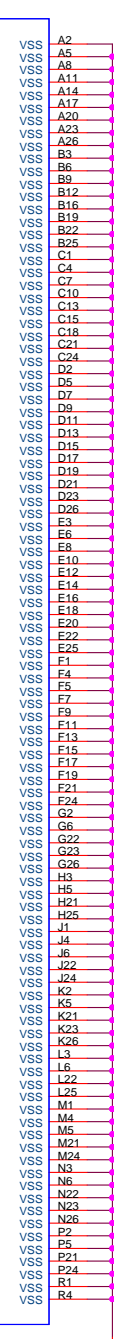
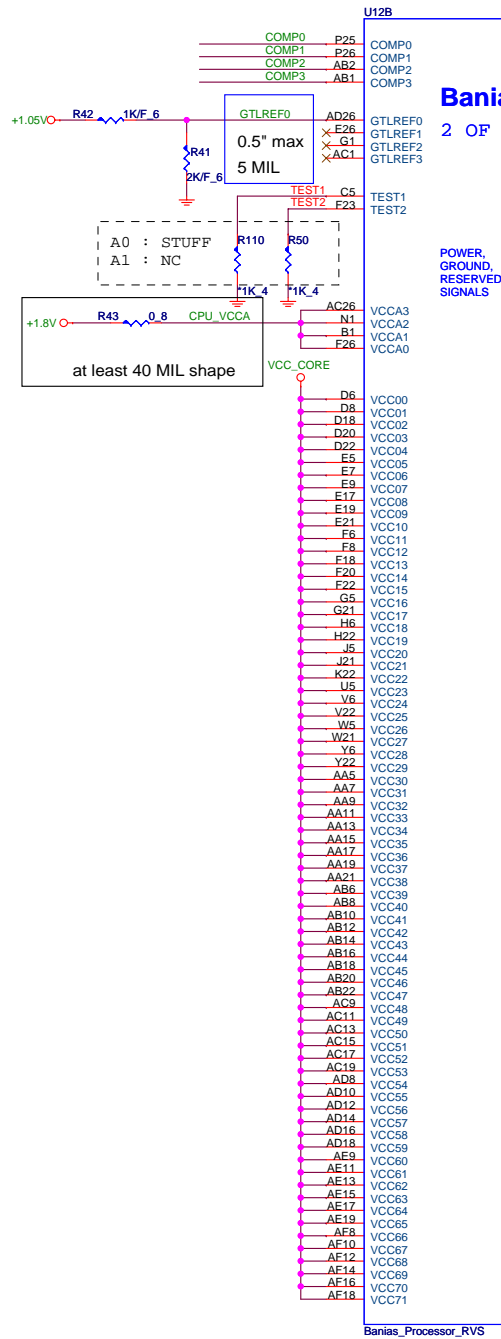
The diagram shows the internal circuitry of the PWROK signal. The PWROK signal from the (6,12,23) connector is pulled up to +3VPCU by resistor R366 (4.7K) and connected to resistor R92 (330). This network drives the base of PNP transistor Q7 (MMB53904), whose emitter is at +3VPCU. The collector of Q7 is connected to the THER\_OVT# signal line via resistor R74 (0.6), which then connects to the 8744\_SHT# pin (pin 26) of the 8744 connector.



CPU



COMP0 ~ 4 max length 500 MIL





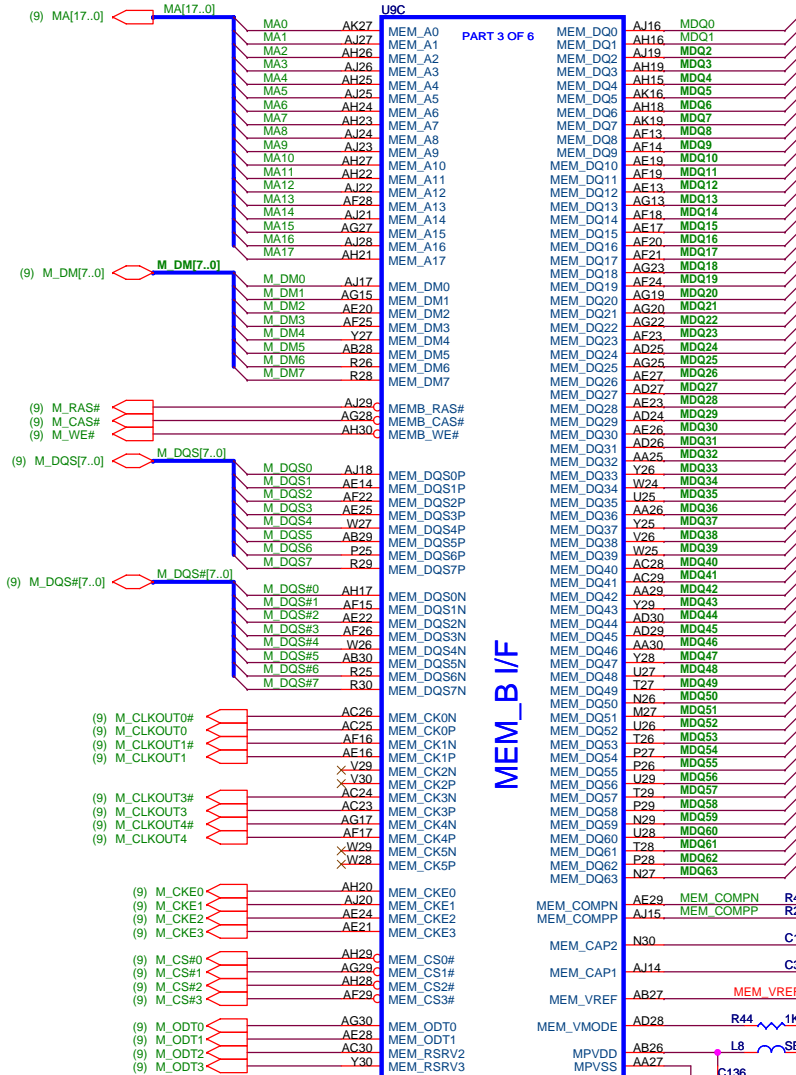
CLG

RC410MB  
MPVSS need to connect to GND plane  
immediately through  
a dedicated VIA

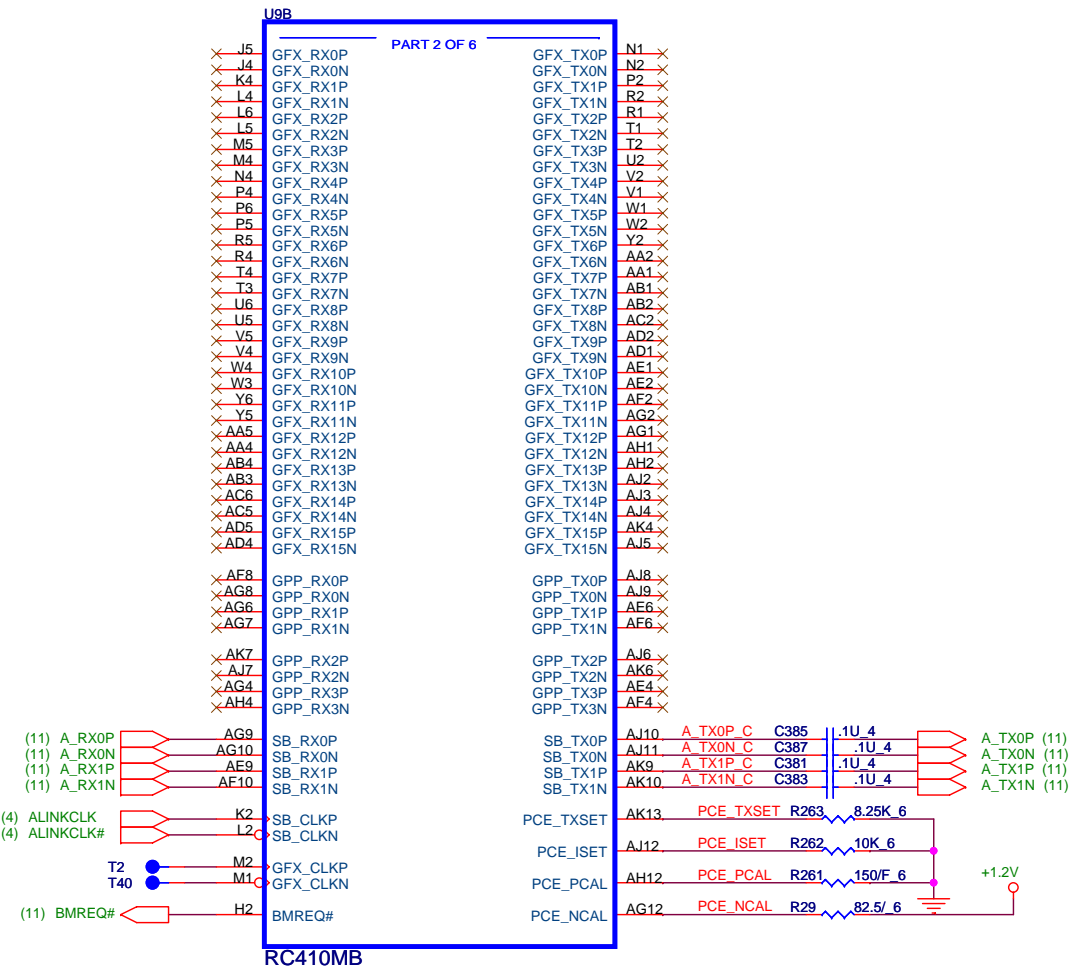
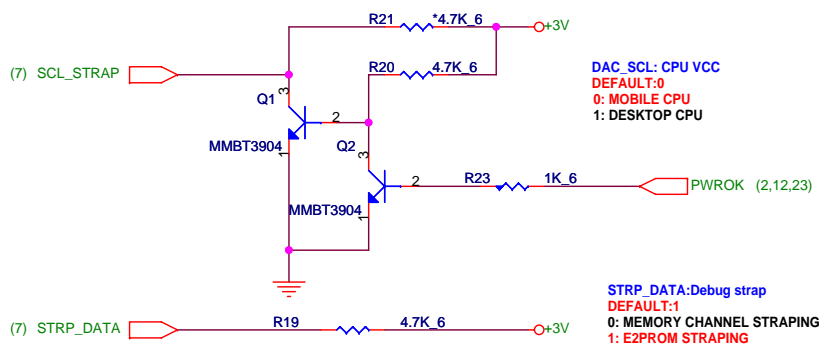
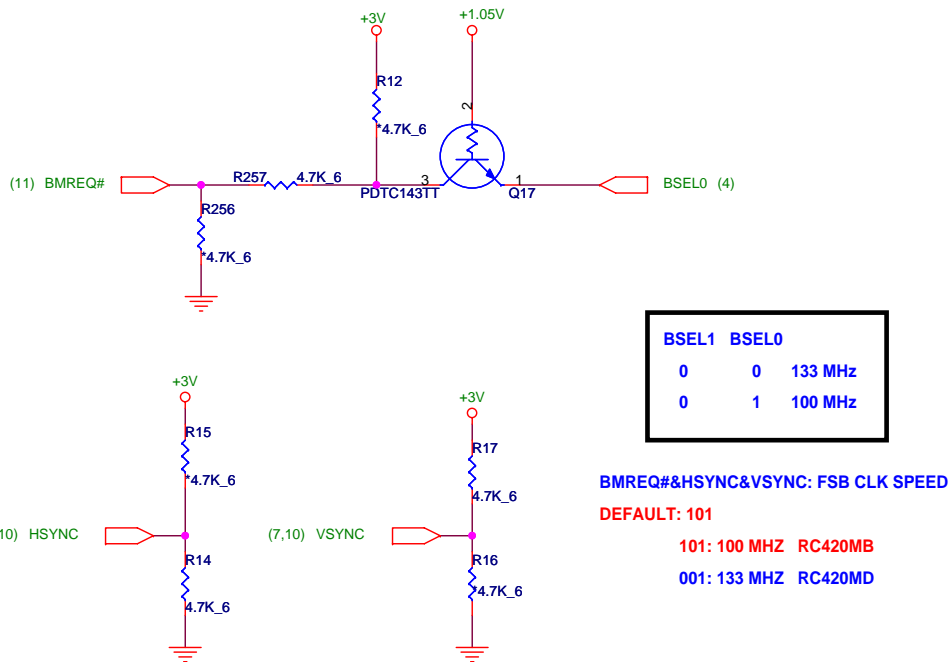
MEM\_B I/F


PART 3 OF 6

U8C



# NB strapping



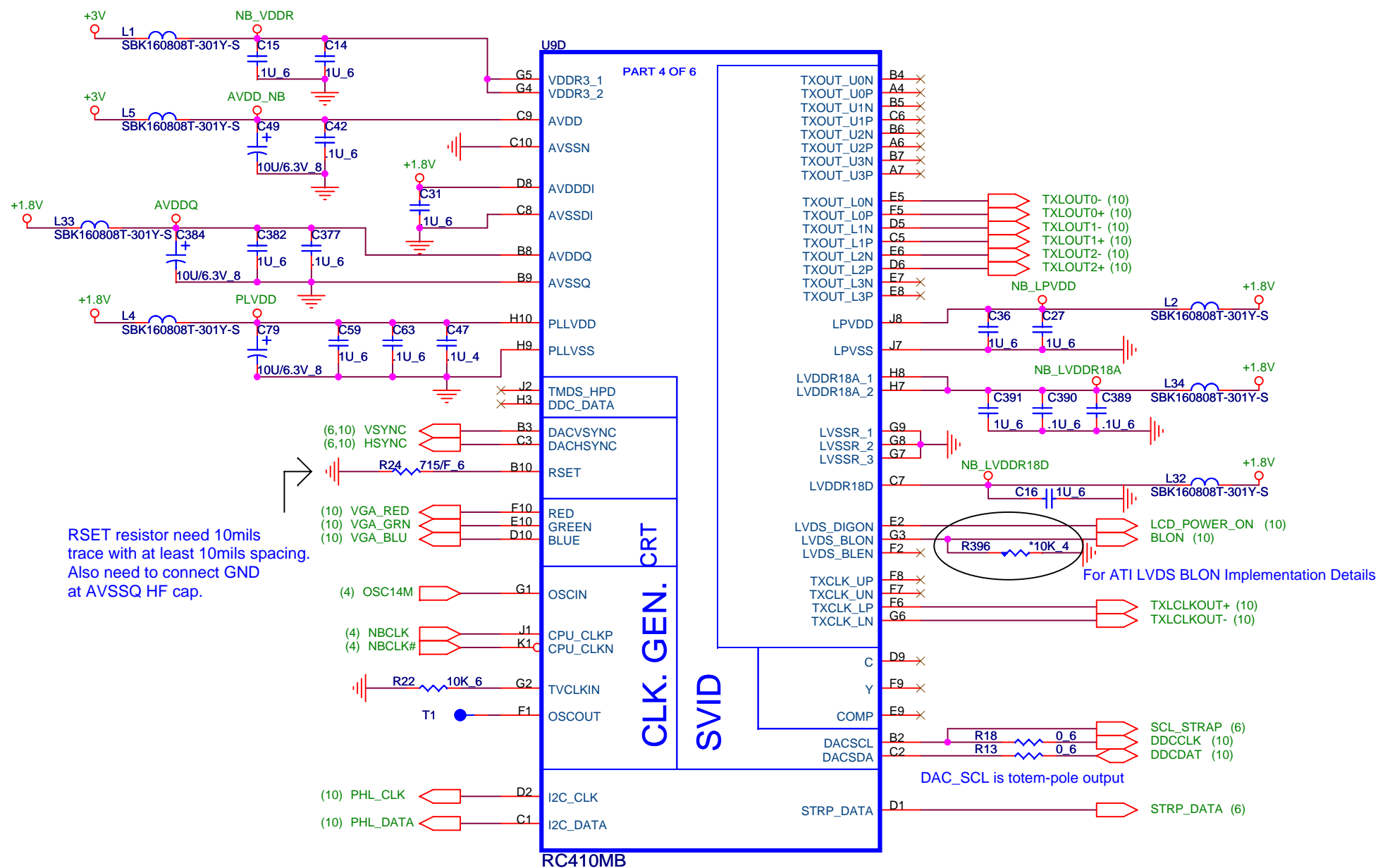


PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A
Date:	Friday, April 28, 2006	Sheet 6 of 30

# CLG

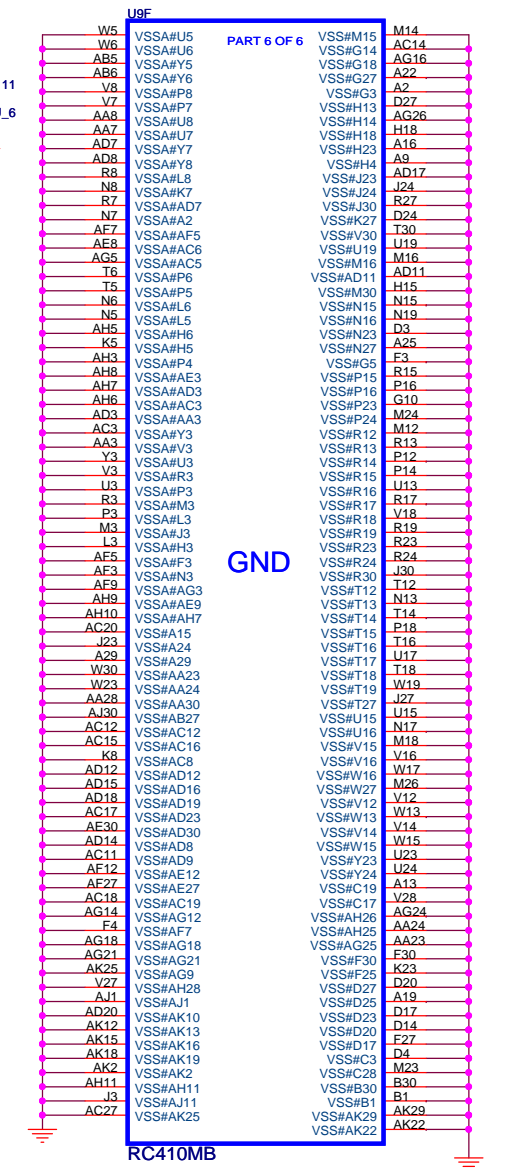
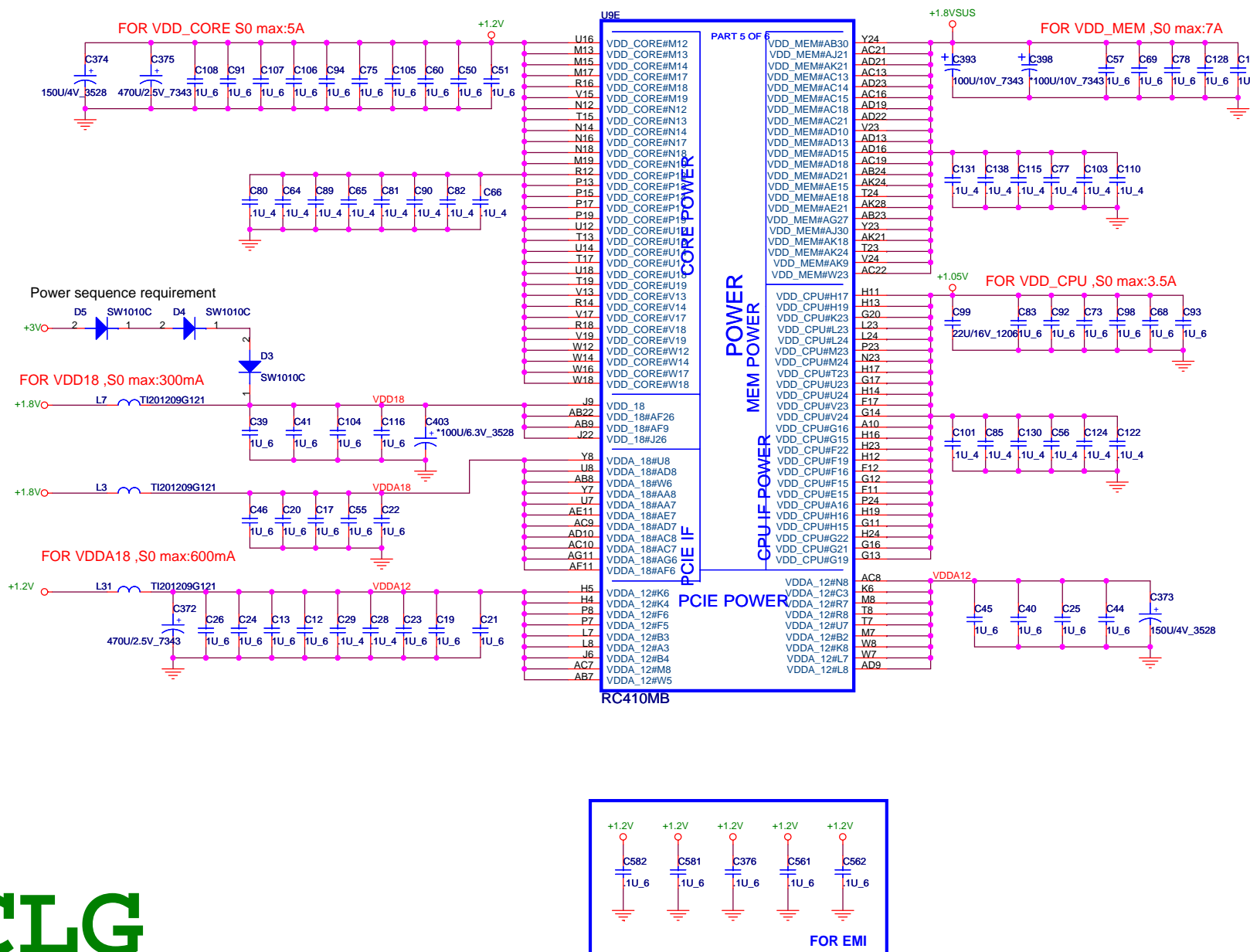


**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-VIDEO &amp; CLKGEN</b>	2A
Date:	Friday, May 05, 2006	Sheet 7 of 30



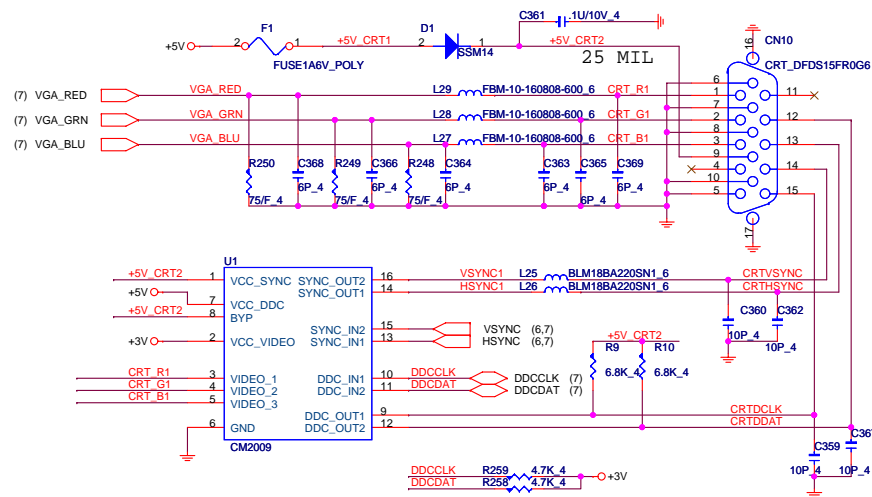
CLG



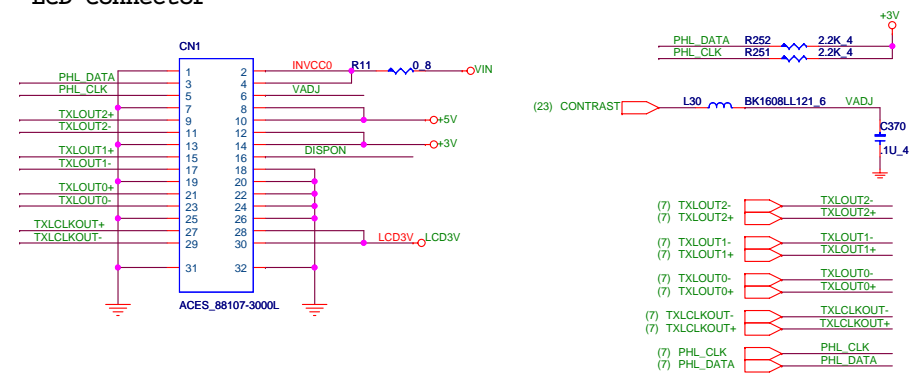




## CRT PORT

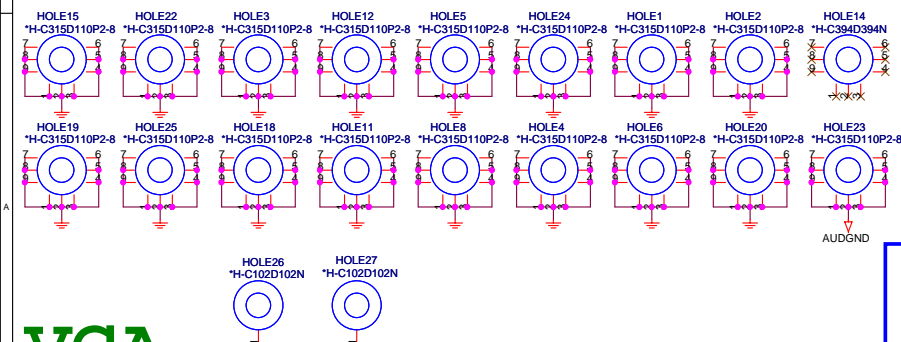
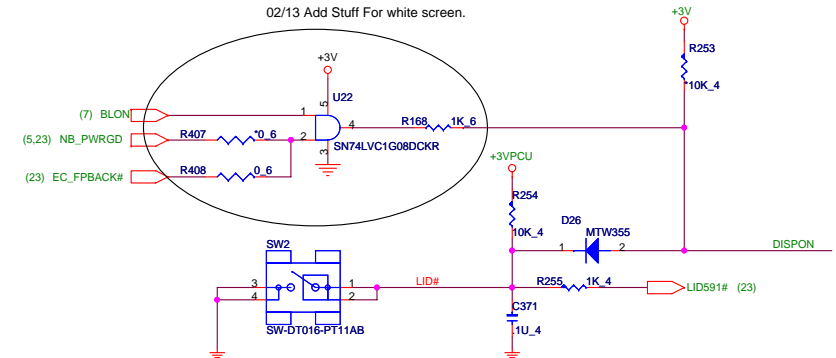


## LCD Connector



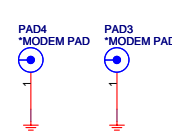
## Lid Switch

05/05 Add Resistor 1Kohm on Buffer output.  
04/28 The Solve Boot up white line on LG LCD issue.  
02/13 Add Stuff for white screen.

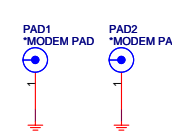


3/31 Add EMI Solution

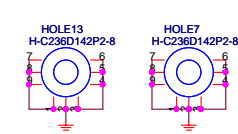
## EMI PAD



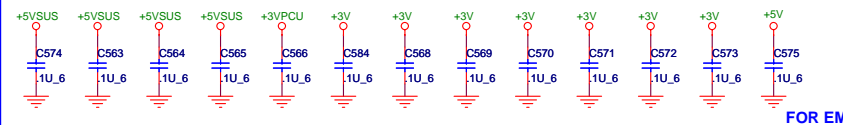
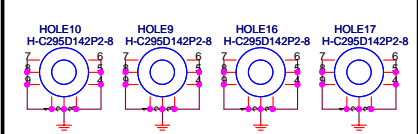
## Modem



## NB SINK



## CPU SINK

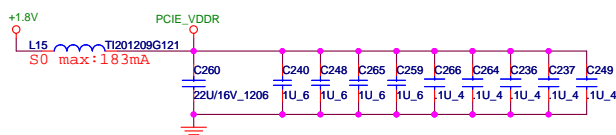


FOR EMI



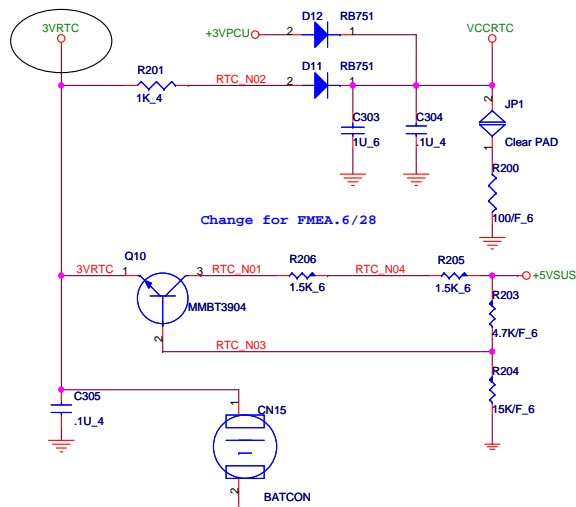
PROJECT : BL1  
Quanta Computer Inc.

Size Document Number  
VGA Ports, LID, & HOLES  
Date: Wednesday, May 10, 2006 Sheet 10 of 30

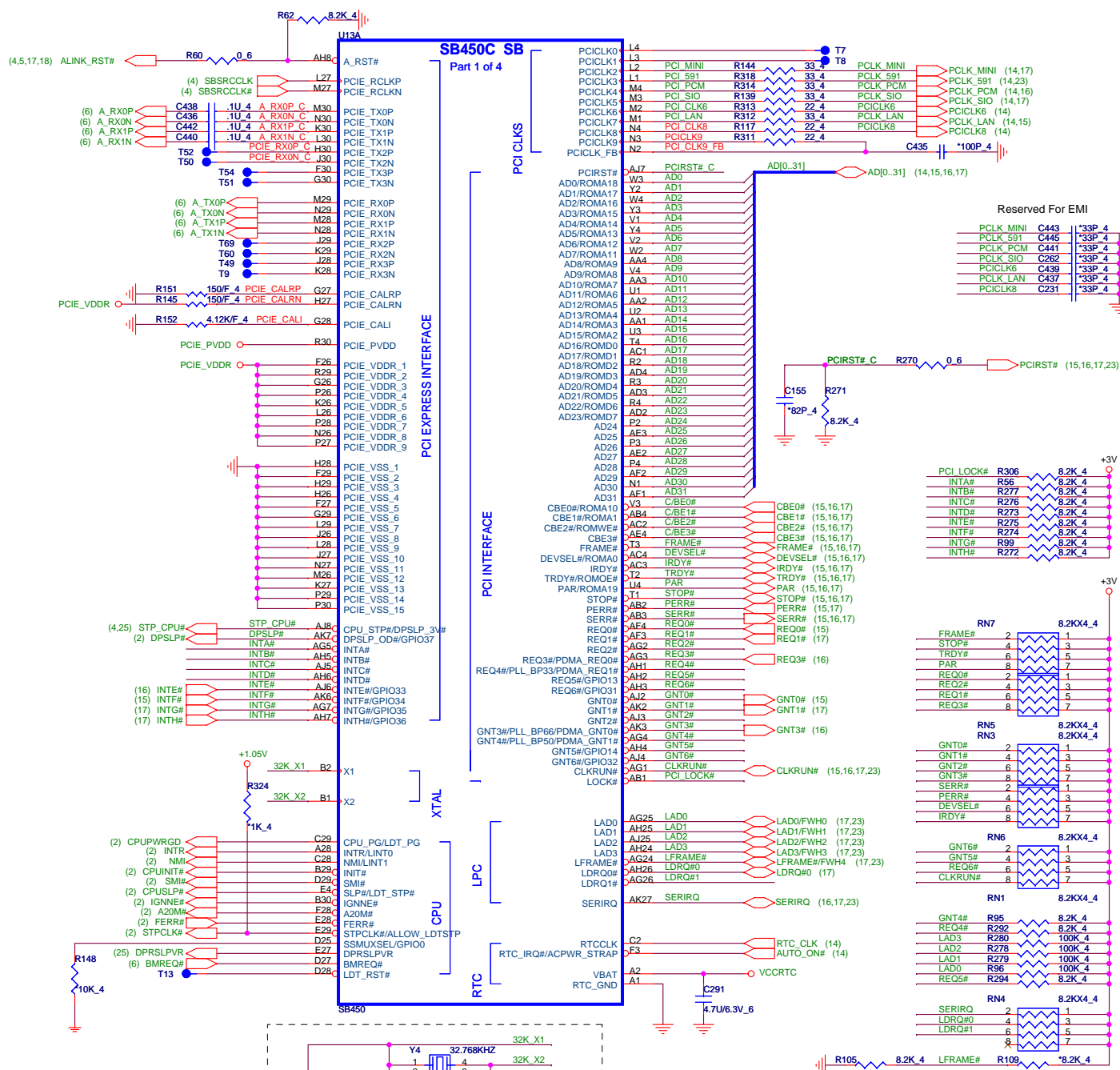


***RTC***

4/2 Battery should be connected directly - not through a UL resistor, and not through a diode.



Change for FMEA.6/28

**CLG**

Reserved For EMI			
PCLK MINI	C443	*33P	4
PCLK 591	C445	*33P	4
PCLK PCM	C441	*33P	4
PCLK SIO	C262	*33P	4
PICLK6	C439	*33P	4
PCLK LAN	C437	*33P	4
PICLK8	C231	*33P	4

PCI_LOCK#	R306	8.2K	4
INTA#	R56	8.2K	4
INTB#	R277	8.2K	4
INTC#	R276	8.2K	4
INTD#	R273	8.2K	4
INTE#	R275	8.2K	4
INTF#	R274	8.2K	4
INTG#	R99	8.2K	4
INTH#	R272	8.2K	4

Signal	Value	Time (ns)
FRAME#	2	0
STOP#	4	0
TRDY#	6	0
PAR	8	0
REQ0#	2	0
REQ2#	4	0
REQ1#	6	0
REQ3#	8	0
FRAME#	2	4
STOP#	4	4
TRDY#	6	4
PAR	8	4
REQ0#	2	4
REQ2#	4	4
REQ1#	6	4
REQ3#	8	4
FRAME#	2	8
STOP#	4	8
TRDY#	6	8
PAR	8	8
REQ0#	2	8
REQ2#	4	8
REQ1#	6	8
REQ3#	8	8

	RNS RN3	8.210K_4 8.210K_4
GNT0#	2	1
GNT1#	4	3
GNT2#	6	5
GNT3#	8	7
SERR#	2	1
PERR#	4	3
DEVSEL#	6	5
IRDY#	8	7

Timing diagram for 8.2KX4\_4. The diagram shows four signals: GNT6#, GNT5#, REQ6#, and CLKRUN#. The signals are plotted against time, with GNT6# and GNT5# showing a series of pulses. REQ6# and CLKRUN# are shown as single pulses. The signals are labeled with their respective pin numbers: 2, 4, 6, 8 for the left side and 1, 3, 5, 7 for the right side.

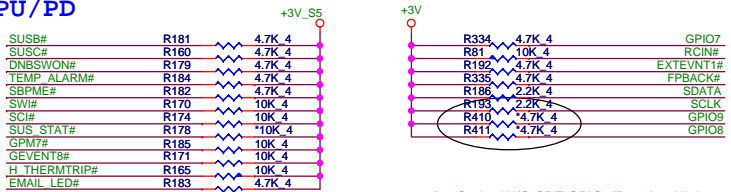
	RN1	8.2KX4_4
GNT4#	R95	8.2K 4
REQ4#	R292	8.2K 4
LAD3	R280	100K 4
LAD2	R278	100K 4
LAD1	R279	100K 4
LAD0	R96	100K 4
REQ5#	R294	8.2K 4



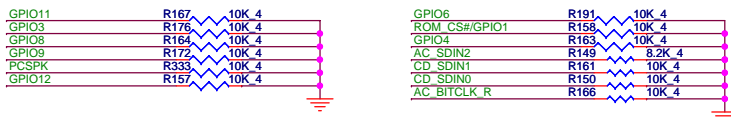
PROJECT : BL1  
Quanta Computer Inc.

Size Custom	Document Number <b>SB450C PCIE/PCI/CPU/LPC I/F</b>	Rev <b>1A</b>
Date:	Friday, May 05, 2006	Sheet 11 of 30

PU / PD

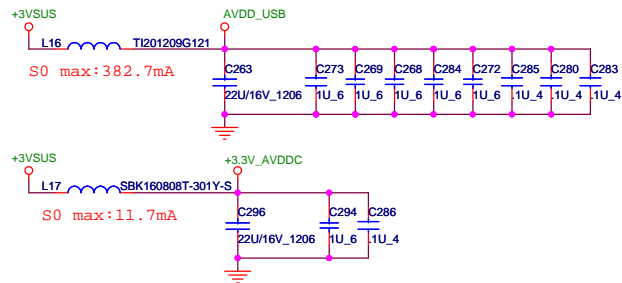
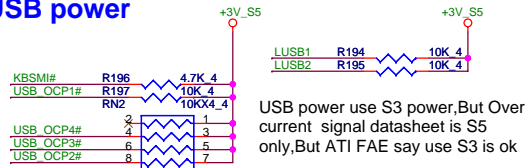
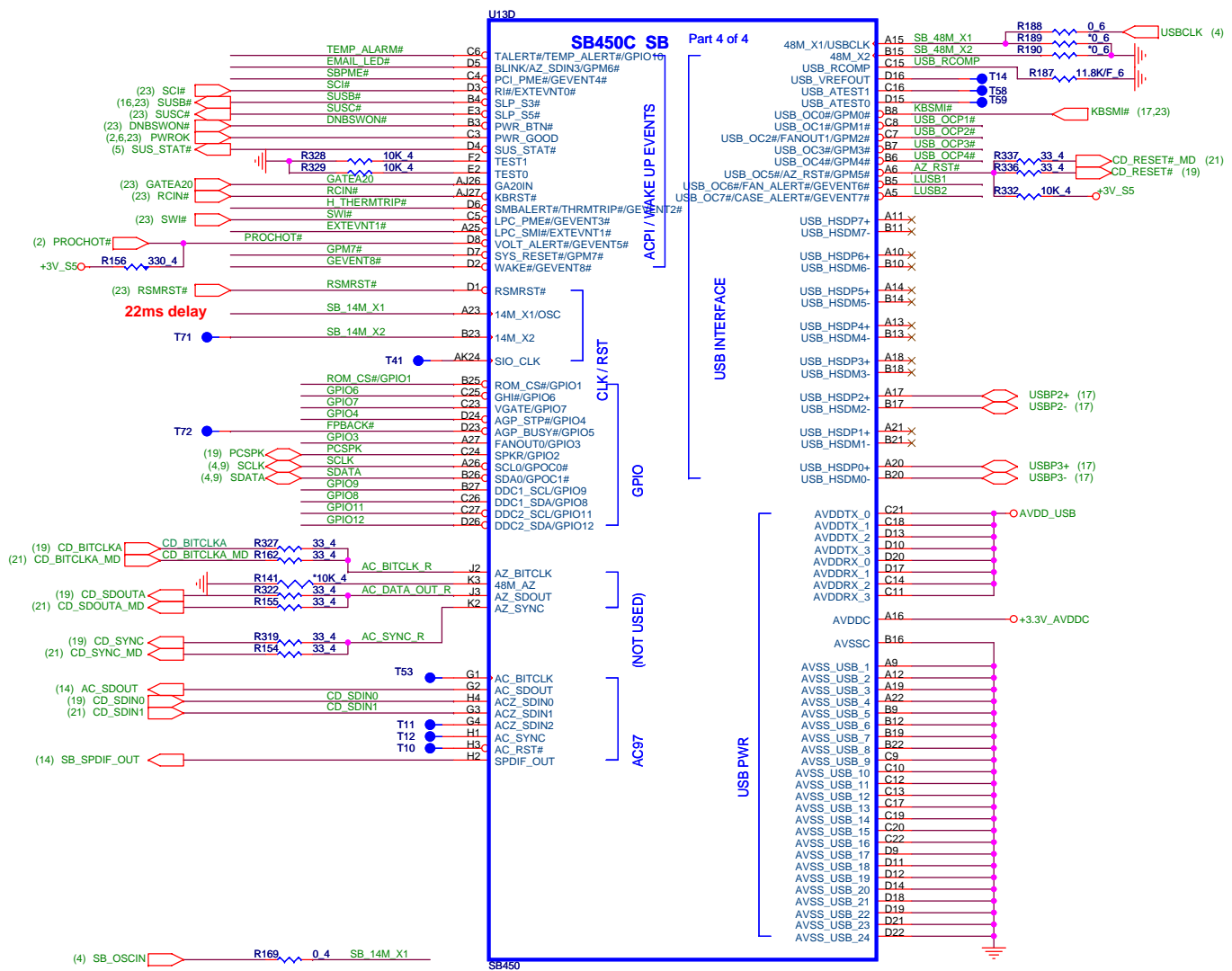


4/02 Option W/O CRT GPIO9(R410) to High.  
4/02 Option(Normal) CRT GPIO9(R172) to Low.



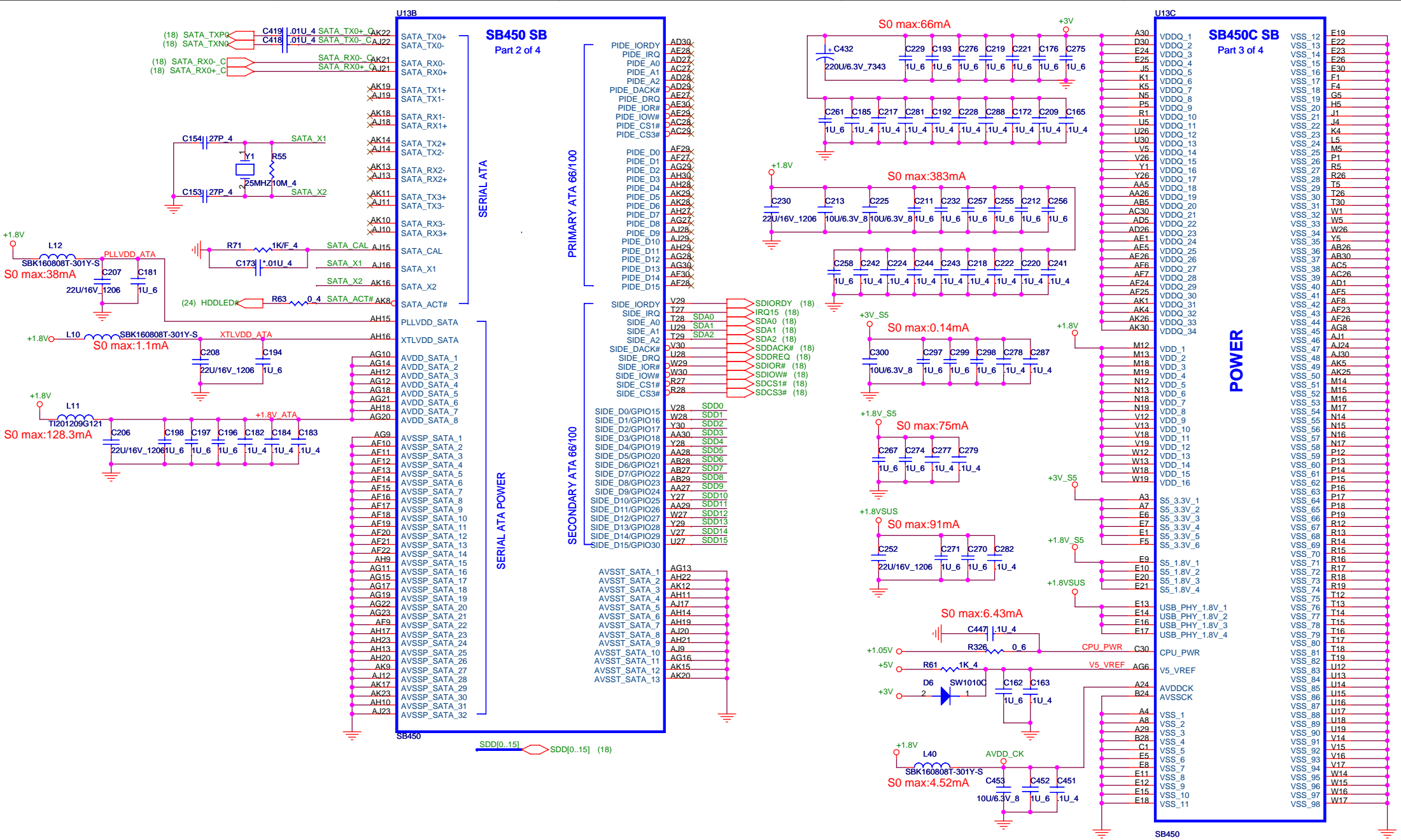
	GPIO9 PIN	GPIO8 PIN
CRT	LOW	
W/O CRT	HIGH	
Modem		LOW
W/O Modem		HIGH

## USB power

**CLG**

PROJECT : BL1  
Quanta Computer Inc.

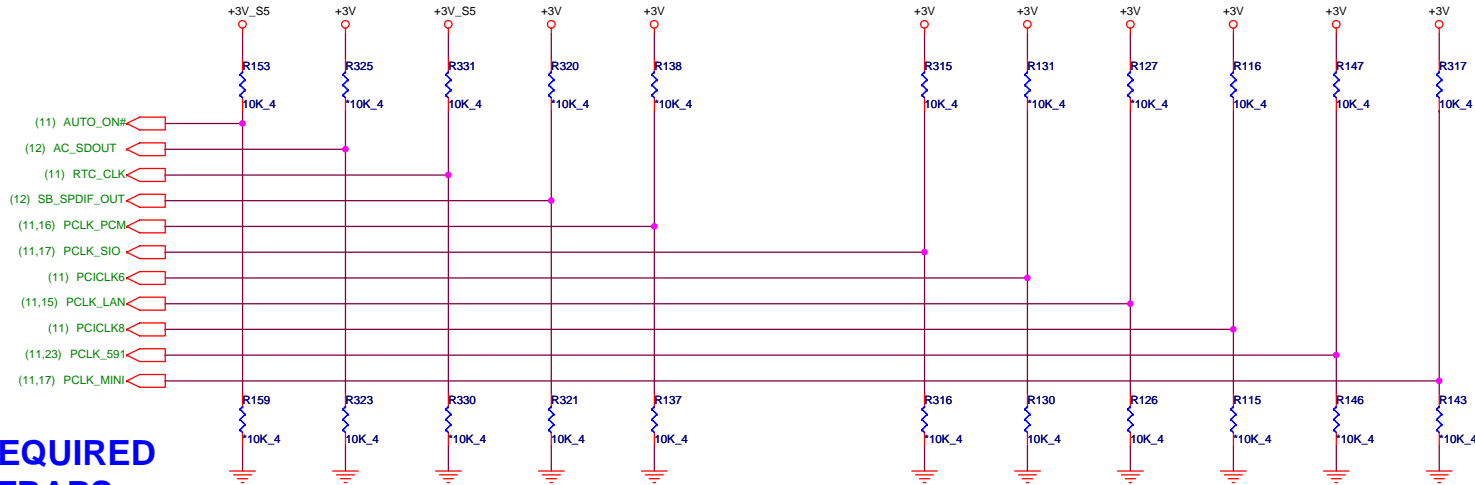
Size Custom	Document Number <b>SB450C ACPI/GPIO/USB/AC97</b>	Rev <b>3A</b>
Date: Monday, May 08, 2006	Sheet 12 of 30	



CLG



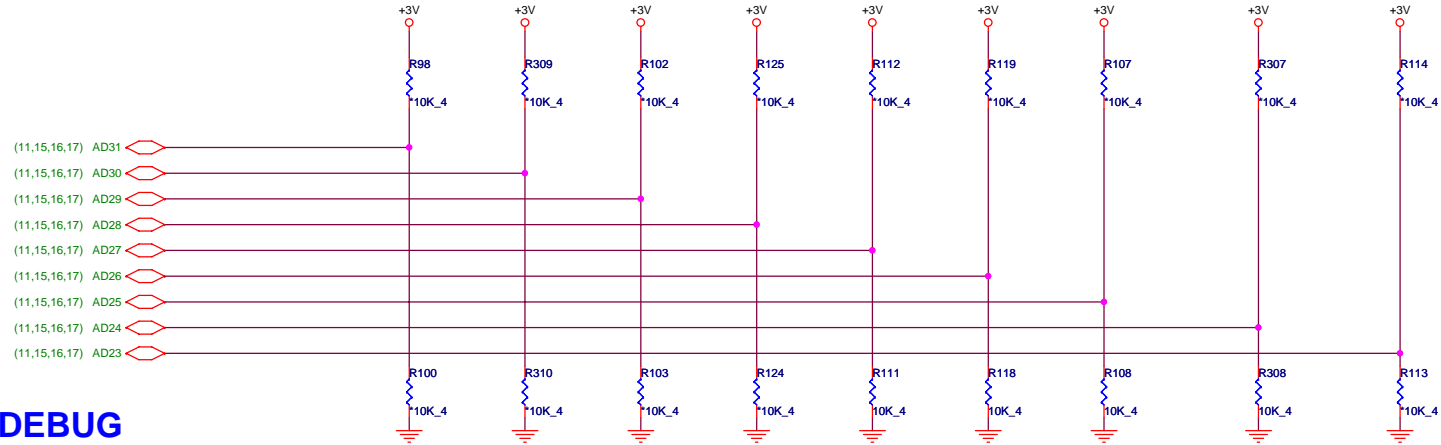
## REQUIRED STRAPS



					PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI*
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE DEFAULT	48MHz Crystal Pad DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712 )	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II (addresses mapped to below 1M) L,L = FWH ROM	DEFAULT	USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.

## DEBUG STRAPS

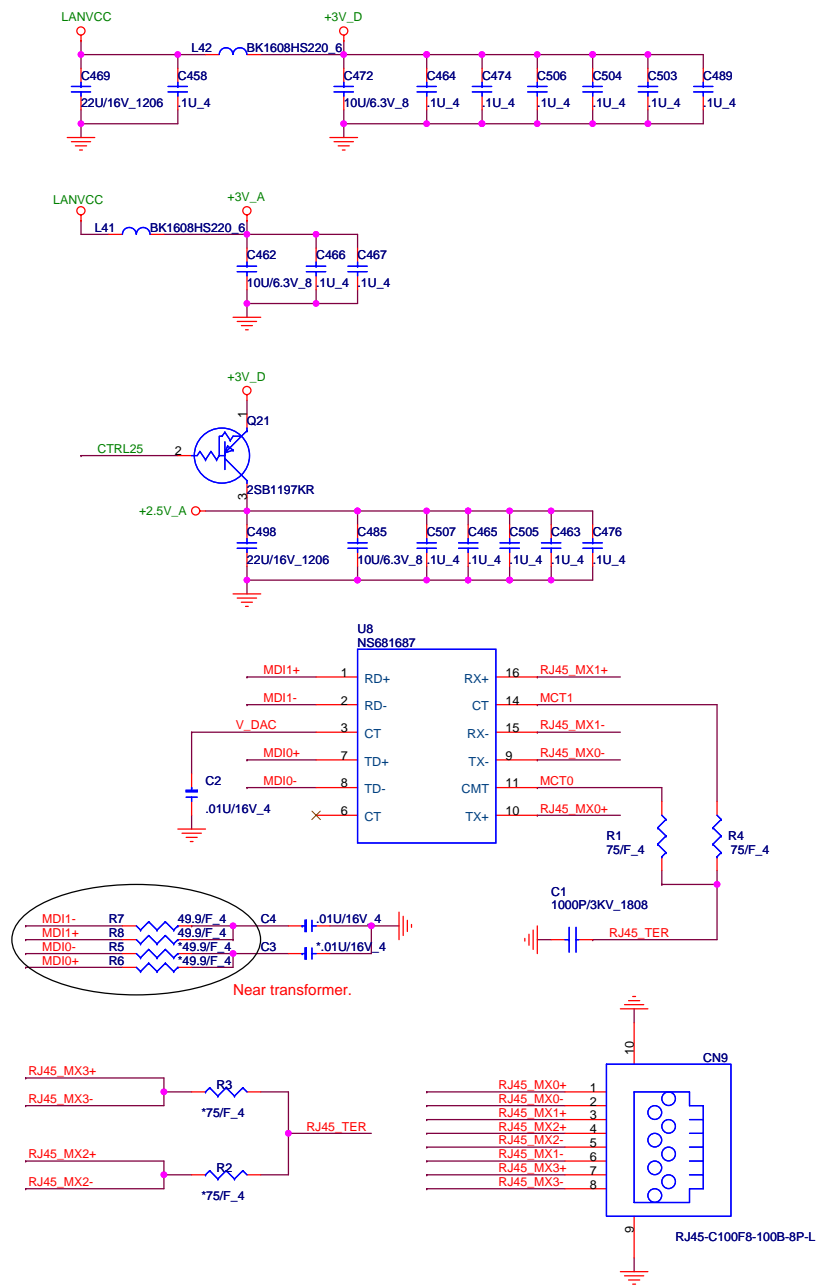
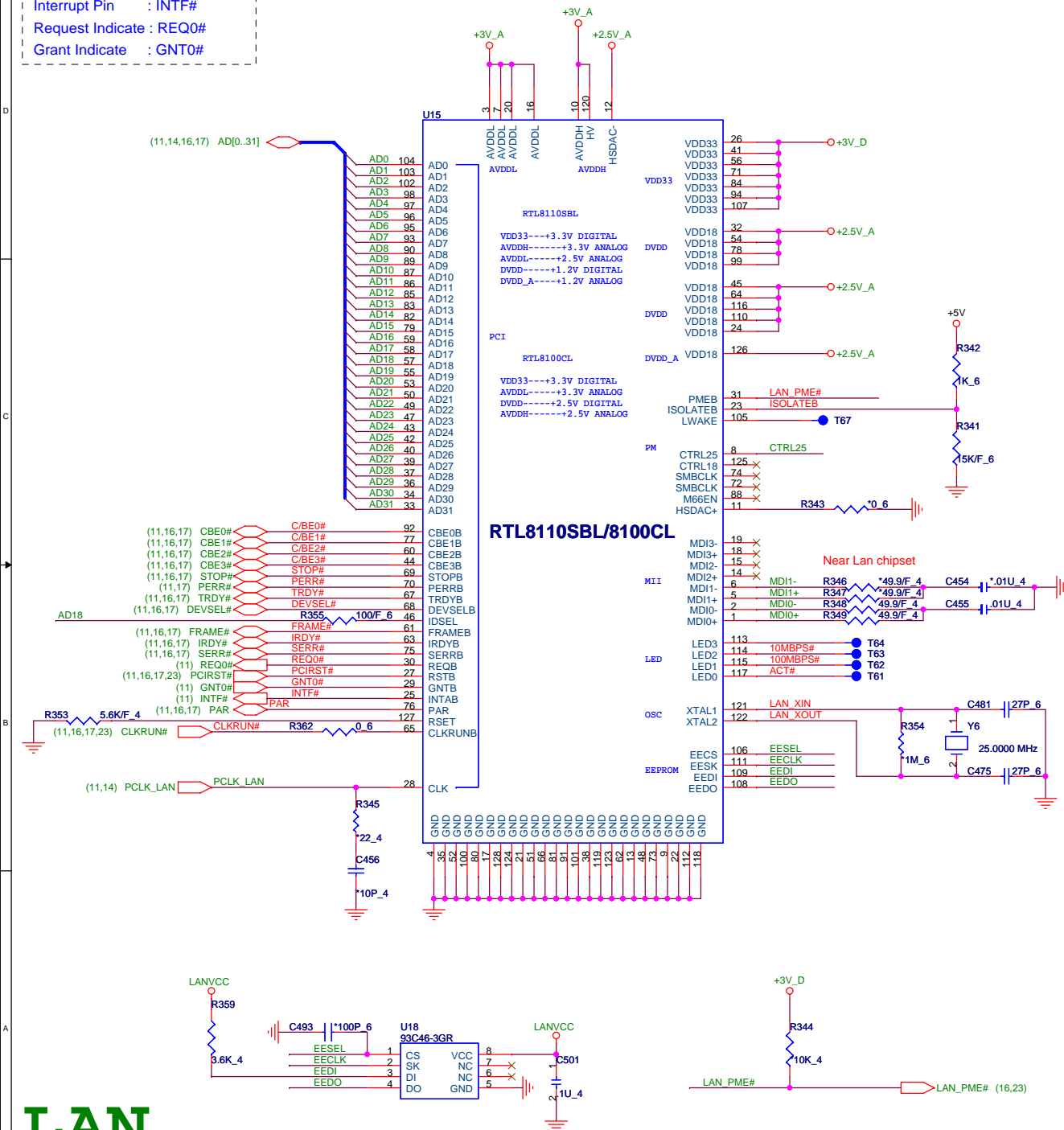



	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

CLG



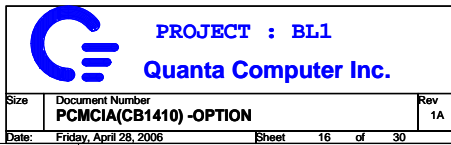
ID Select : AD18  
Interrupt Pin : INTF#  
Request Indicate : REQ0#  
Grant Indicate : GNT0#



 PROJECT : BL1  
Quanta Computer Inc.

Size	Document Number <b>LAN RTL8110SBL/8100CL</b>	Rev <b>1A</b>
Date:	Saturday, May 06, 2006	Sheet 15 of 30

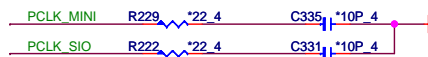
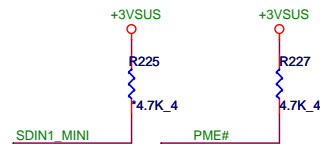
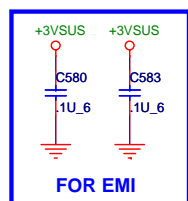
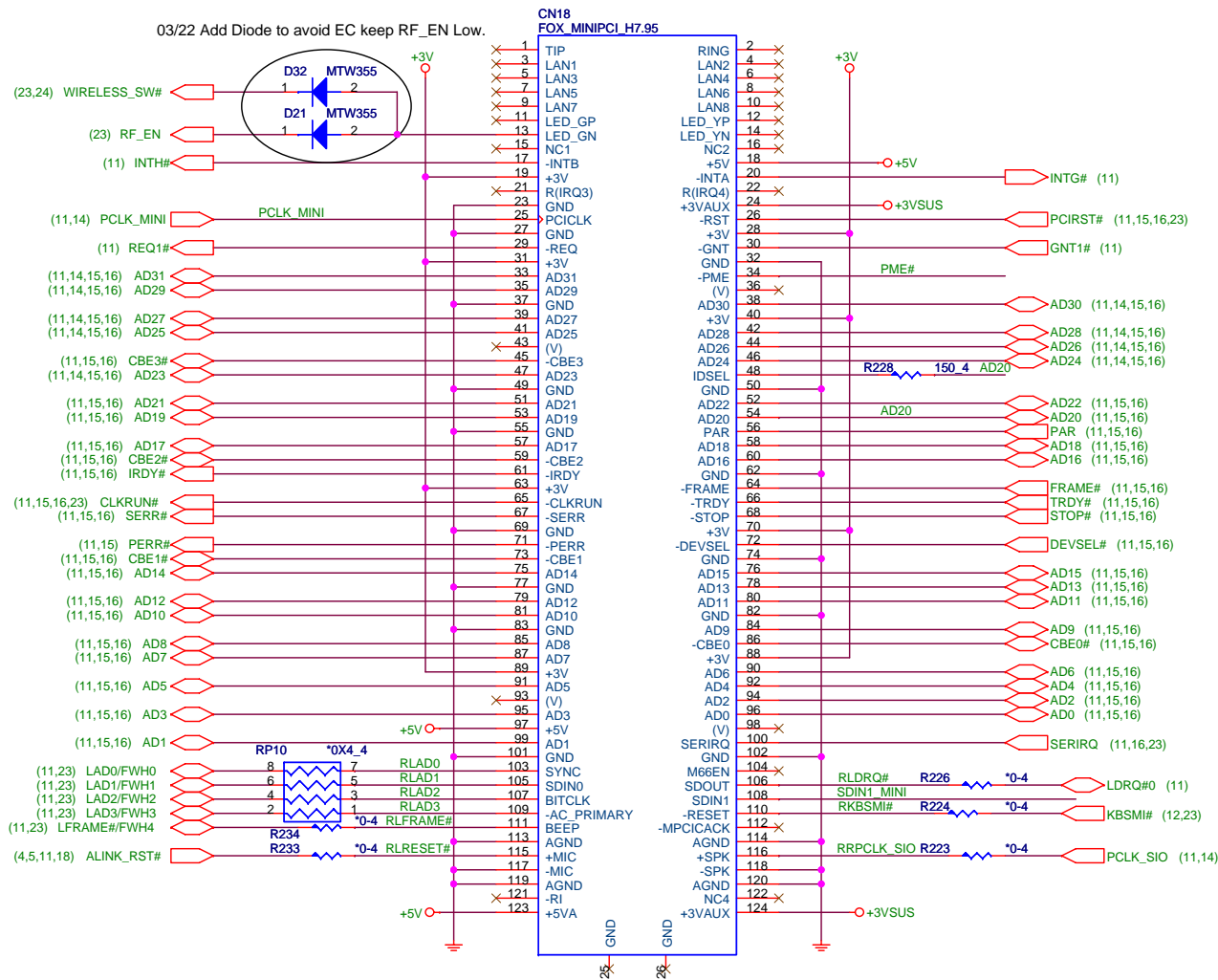
(11,14,15,17) AD[31..0] 



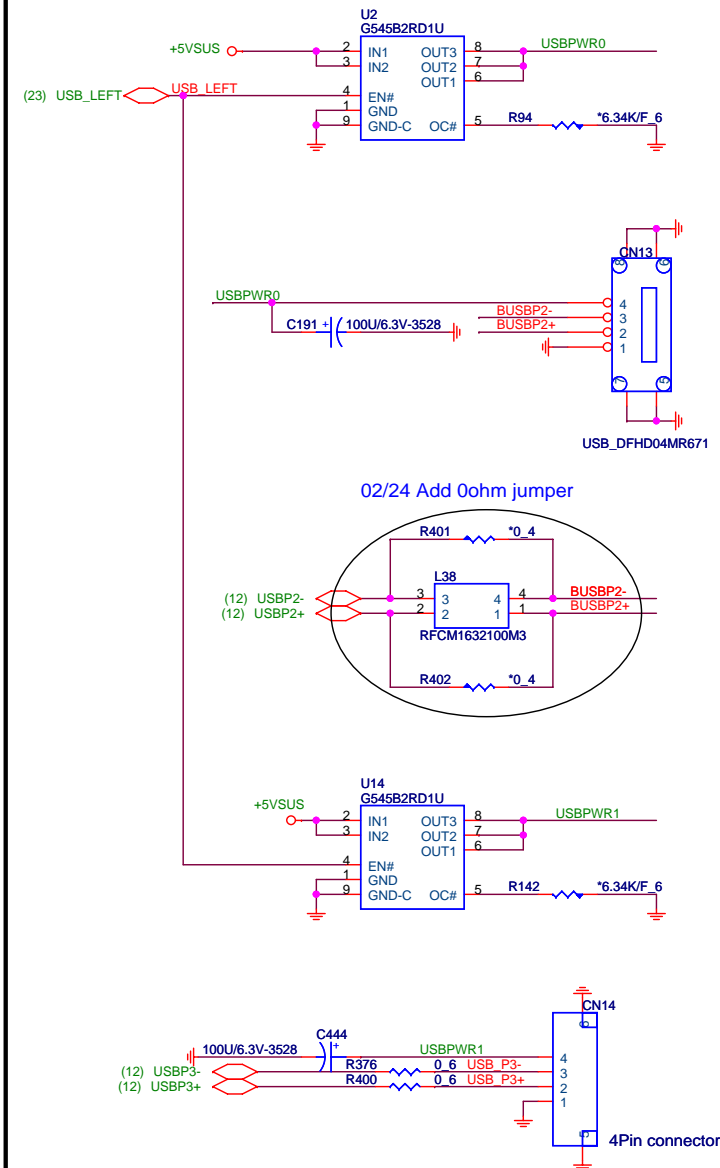
ID Select : AD20  
 Interrupt Pin : INTG# , INT#H  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#

# MINI-PCI

03/22 Add Diode to avoid EC keep RF\_EN Low.



# USB

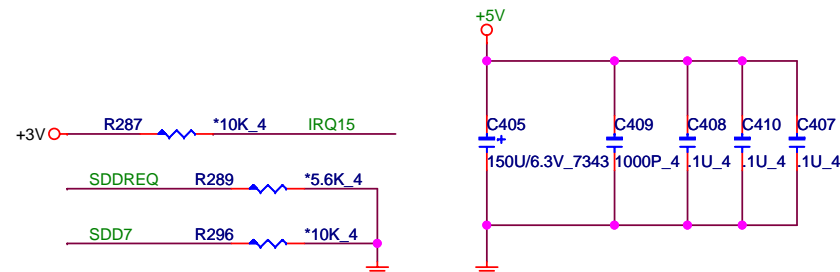
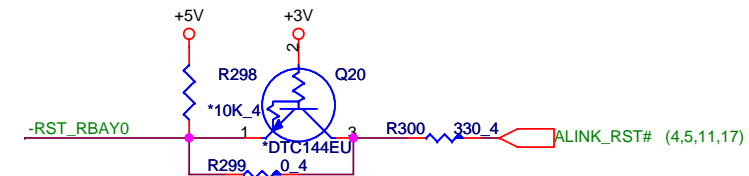
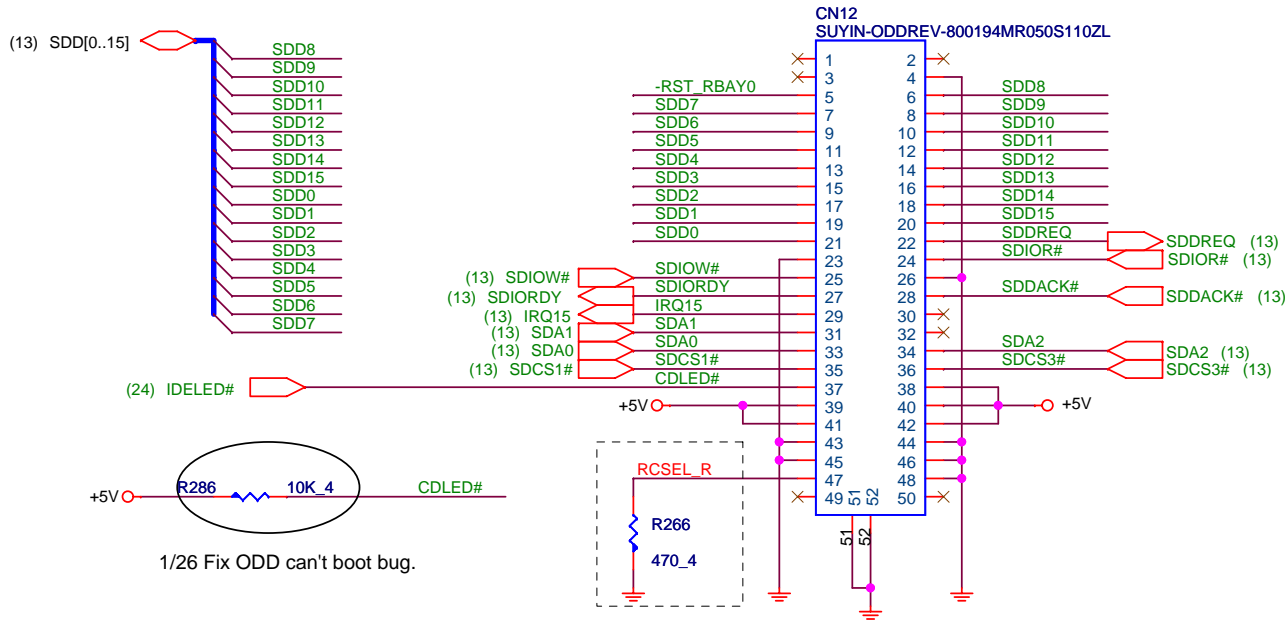


04/28 Del Reserved the Second USB Port.

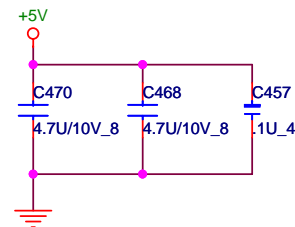
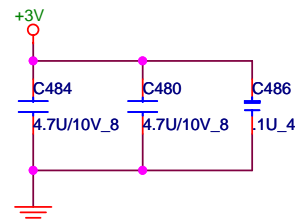
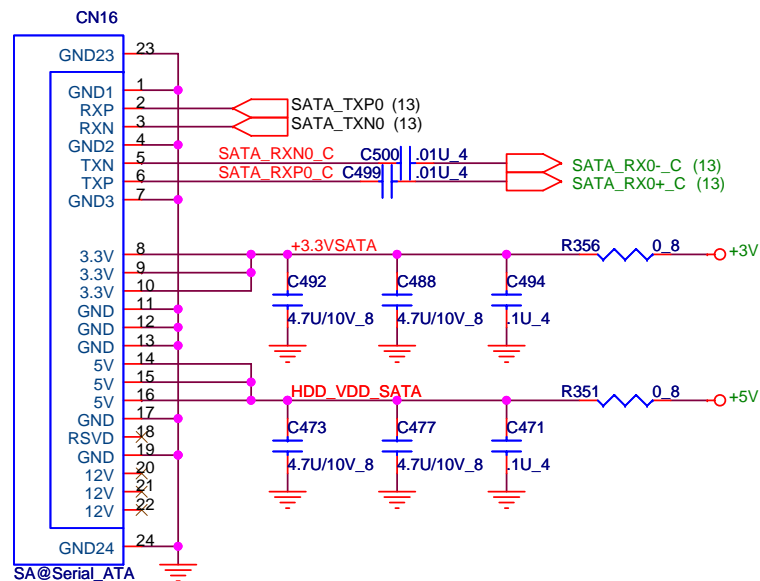


PROJECT : BL1  
 Quanta Computer Inc.

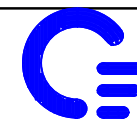
## ODD CONN



## SATA HDD CONN



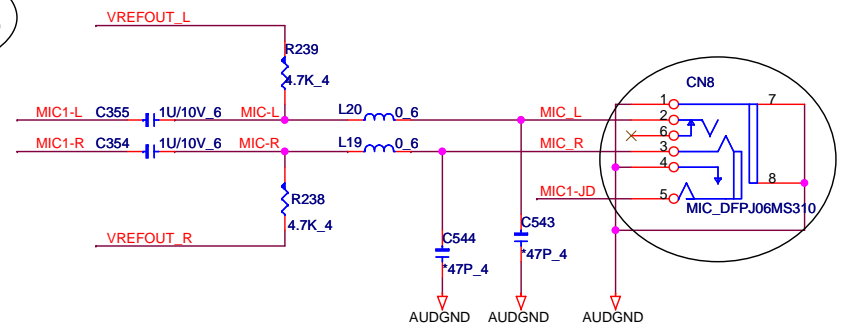
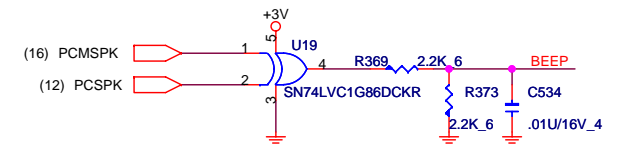
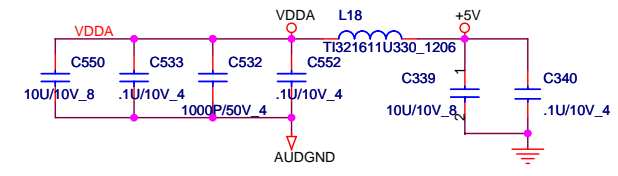
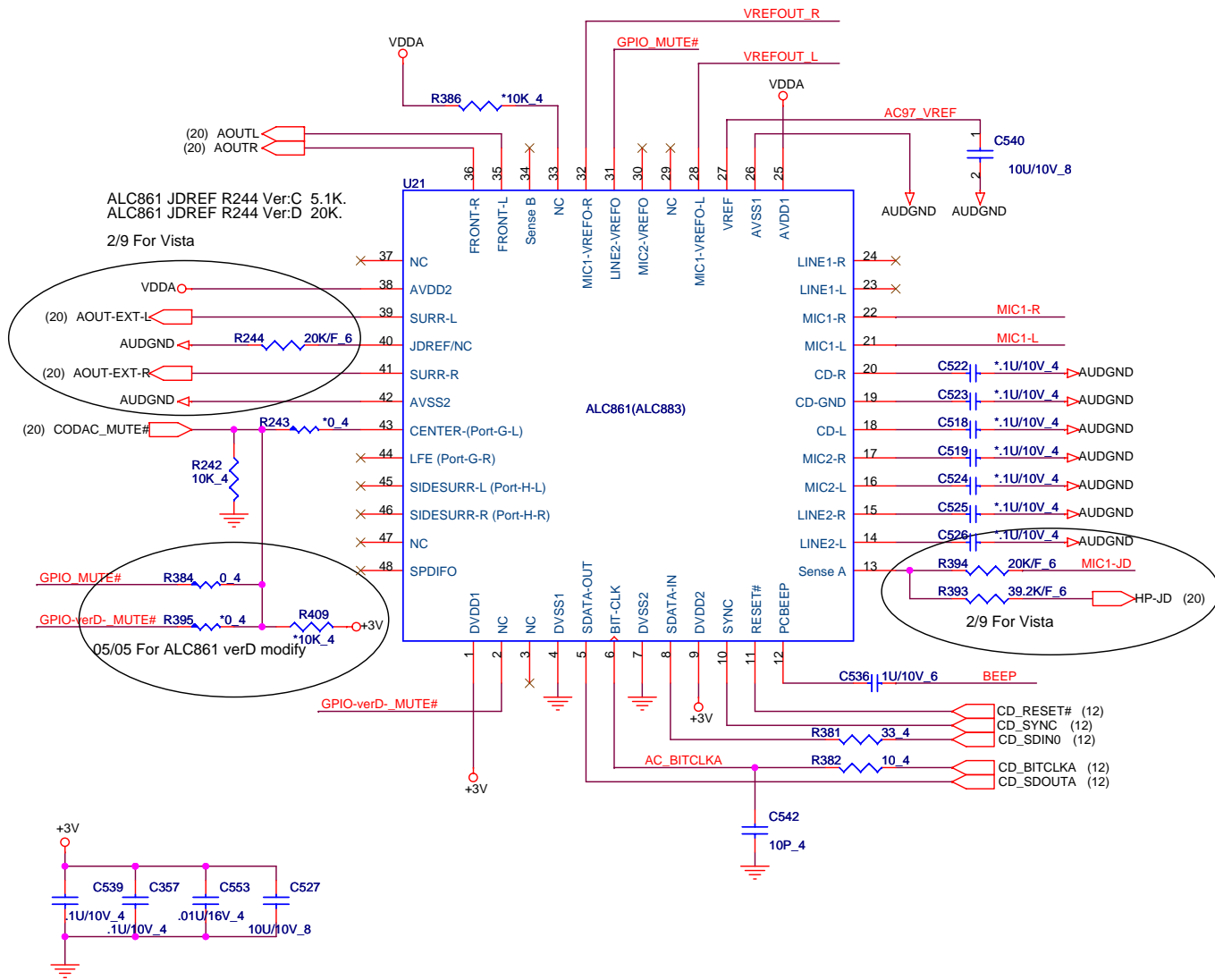
IDE




PROJECT : BL1  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>HDD &amp; CDROM</b>	2A
Date:	Monday, May 08, 2006	Sheet 18 of 30

ADO



Normal Open Jack

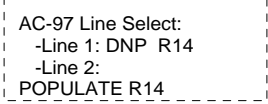


**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>REALTEK ALC861</b>	2A
Date:	Friday, May 05, 2006	Sheet 19 of 30



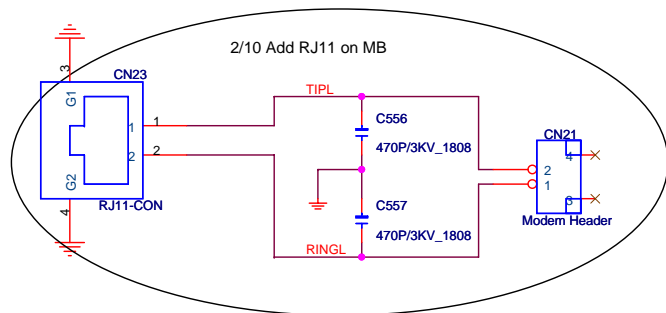




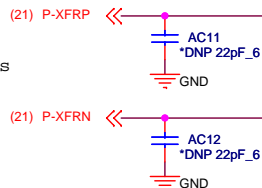
agere<sup>systems</sup>

Title **DELPHI SV92A3 MDC 1.5 Reference Design**

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE



Locate C11, C12 as close to digital device as possible.

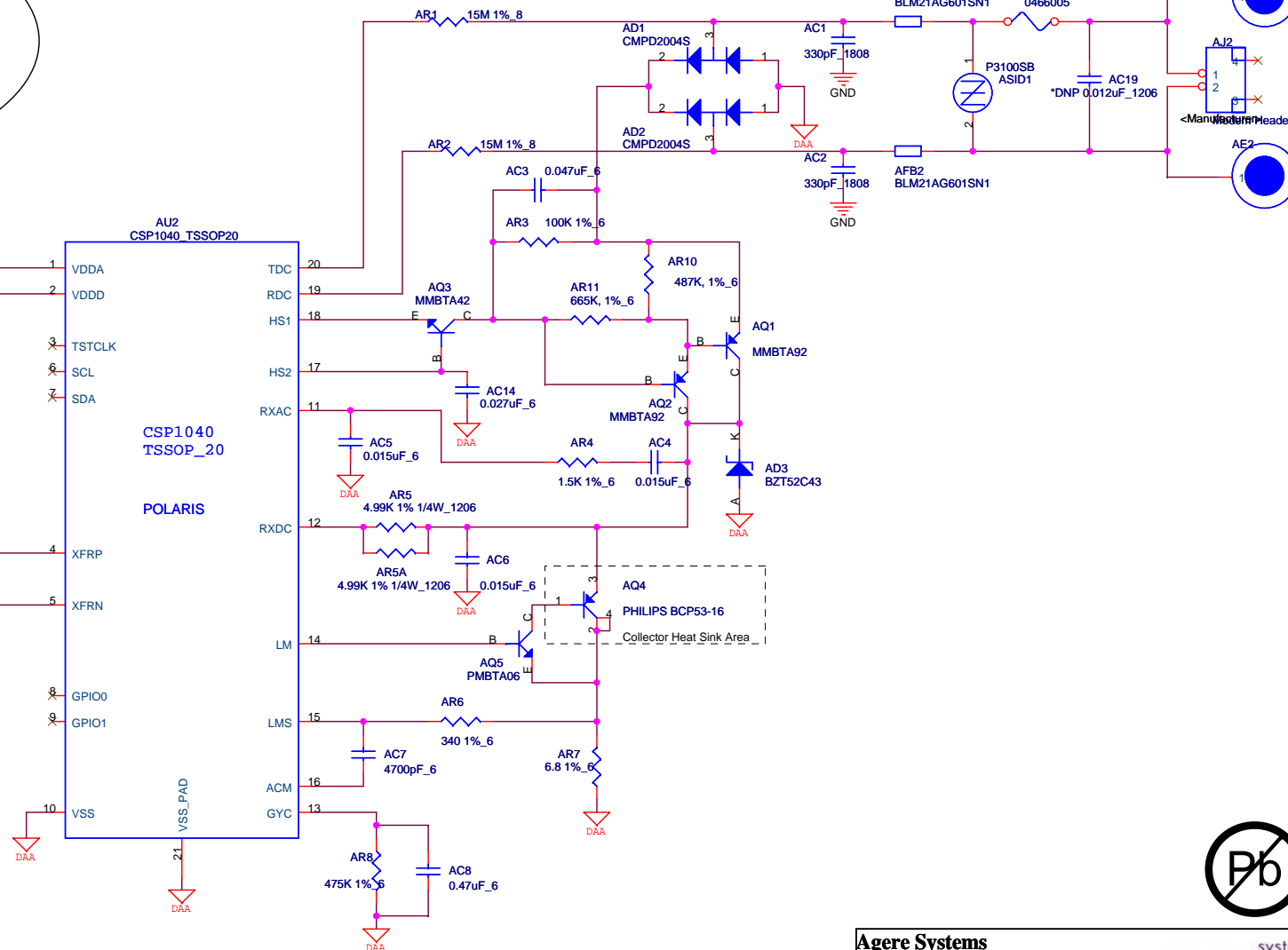


# MDM

## FUSE Note:

The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



<b>Agere Systems</b> Holmdel NJ		
<b>Design Engineer: R. Trevino</b>		
<b>DELPHI SV92A3 MDC 1.5 Reference Design</b>		
Size B	Document Number	Rev 2A
Date:	Saturday, May 06, 2006	Sheet 22 of 30

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE

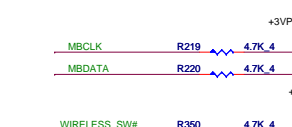
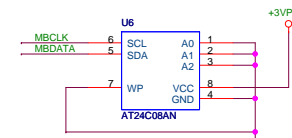
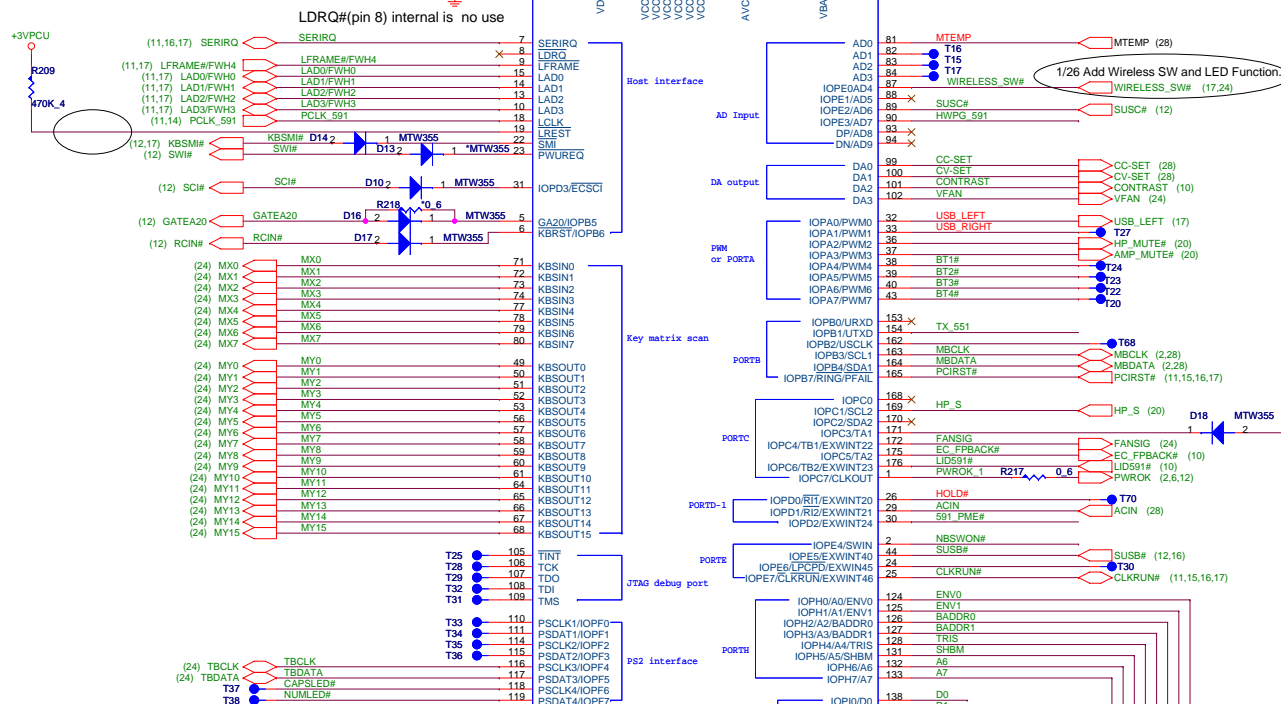
PCLK\_591 R207 \*22.4 C312 \*10P\_4

+3VPCU  
+3V  
C316 1U\_4  
C318 1U\_4  
C302 1U\_4  
C326 1U\_6  
4/02 Change Footprint to 0603.

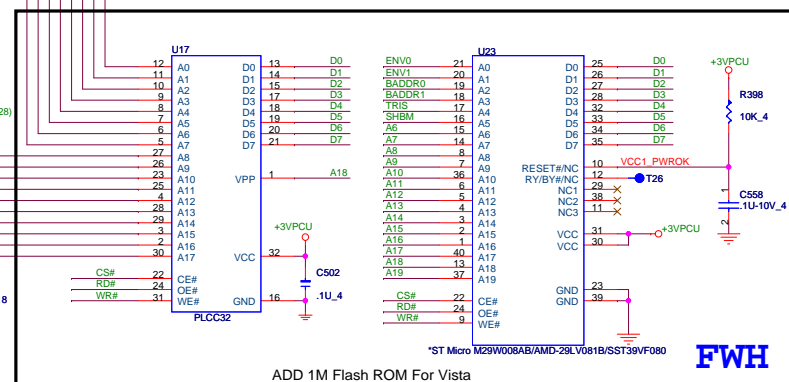
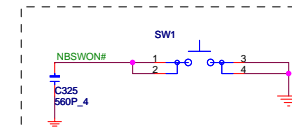
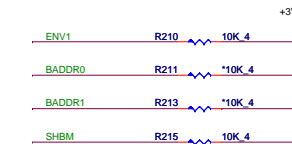
+3VPCU  
C329 10U6.3V\_8  
C322 1U\_4  
C301 1U\_4  
C295 1U\_4  
C328 1U\_4

SRBM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	0E	3F
0 1	4E	4F
1 0	[HCF0BAH, HCF0BAL]	[HCF0BAH, HCF0BAL]+1
1 1		Reserved



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



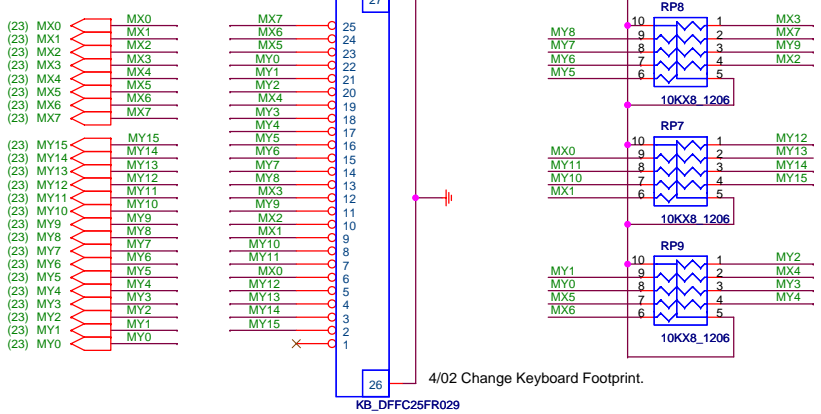
KBC

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	PC97541 & FLASH	2A
Date:	Friday, April 26, 2006	Sheet 23 of 30

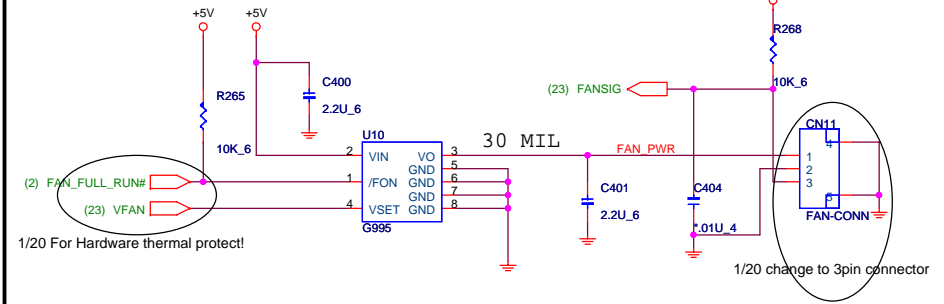
INT K/B



KBC

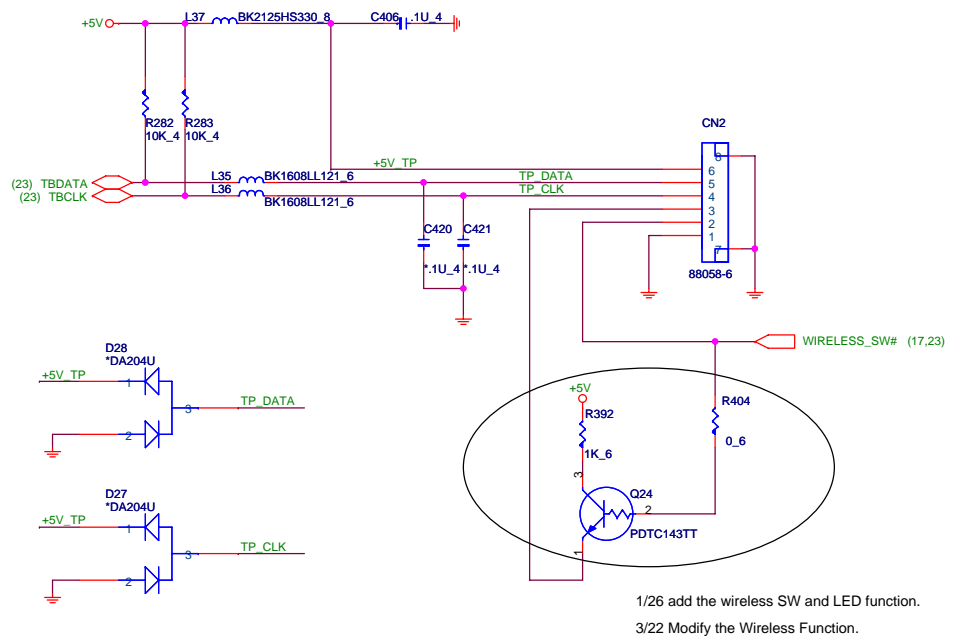
THM

FAN CONTROL



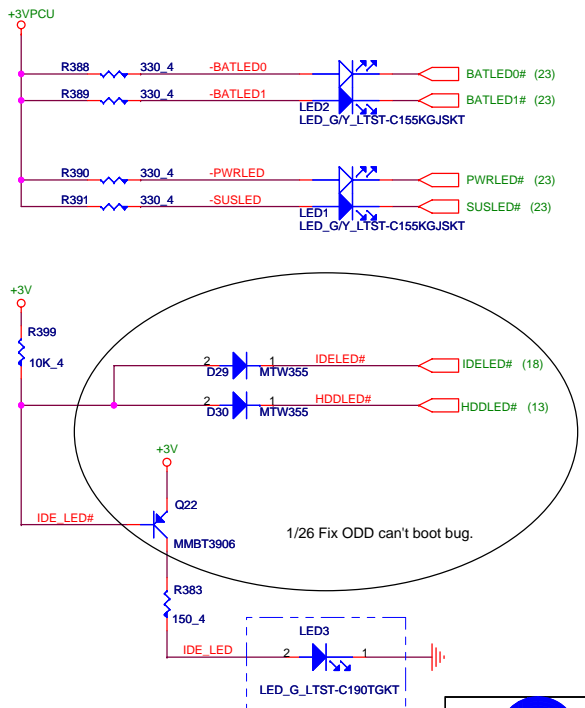
TOUCH PAD

20 MIL

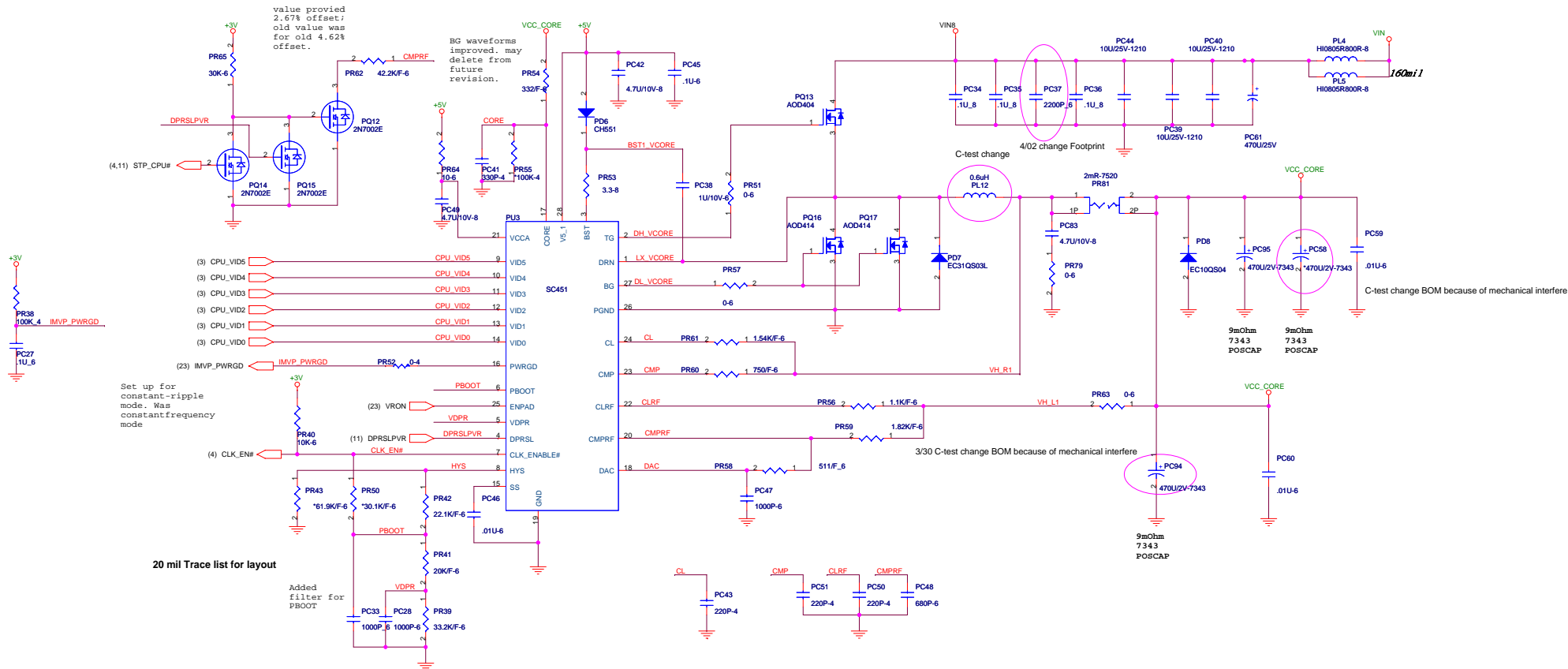


TPD

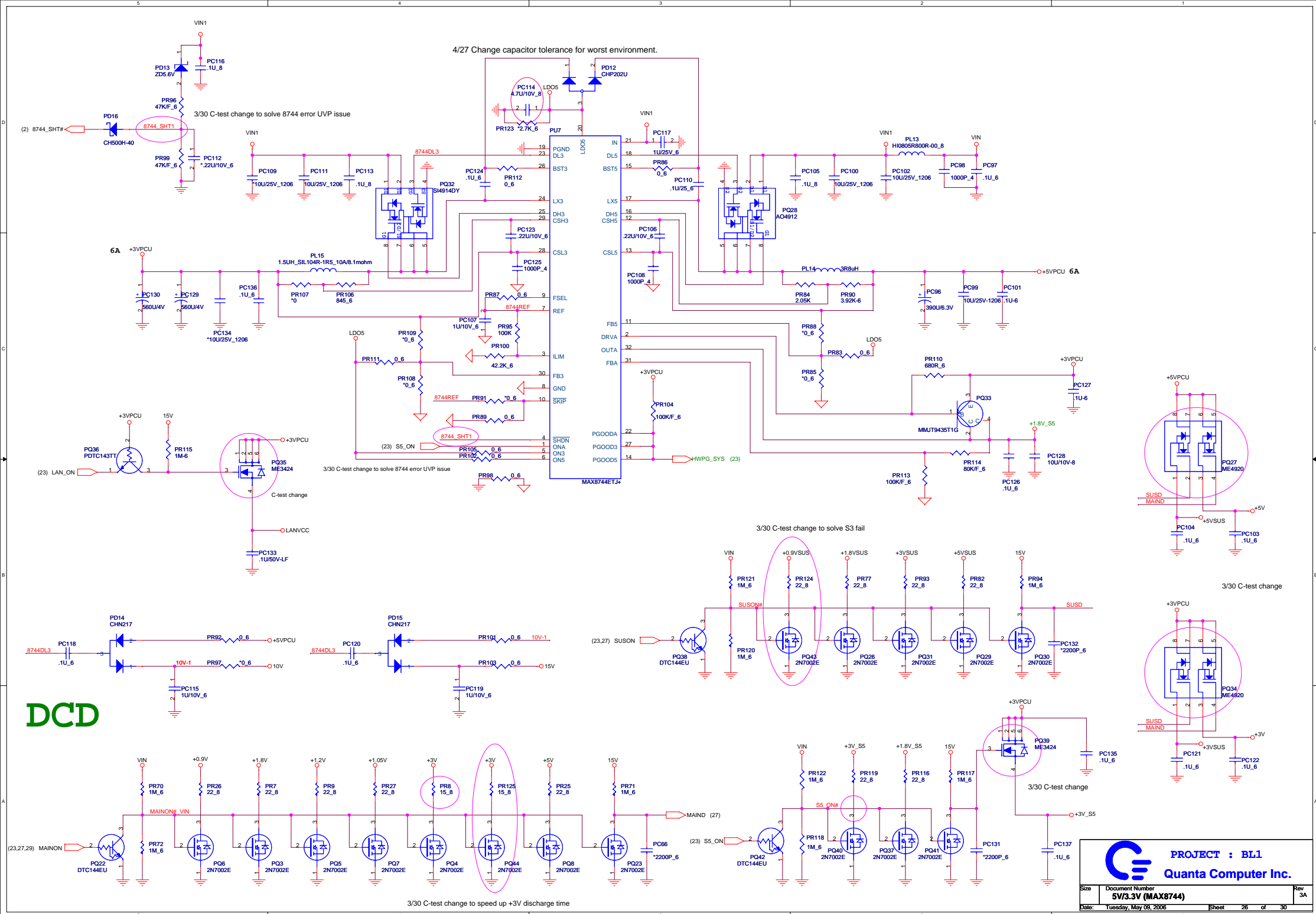
ON BOARD LED



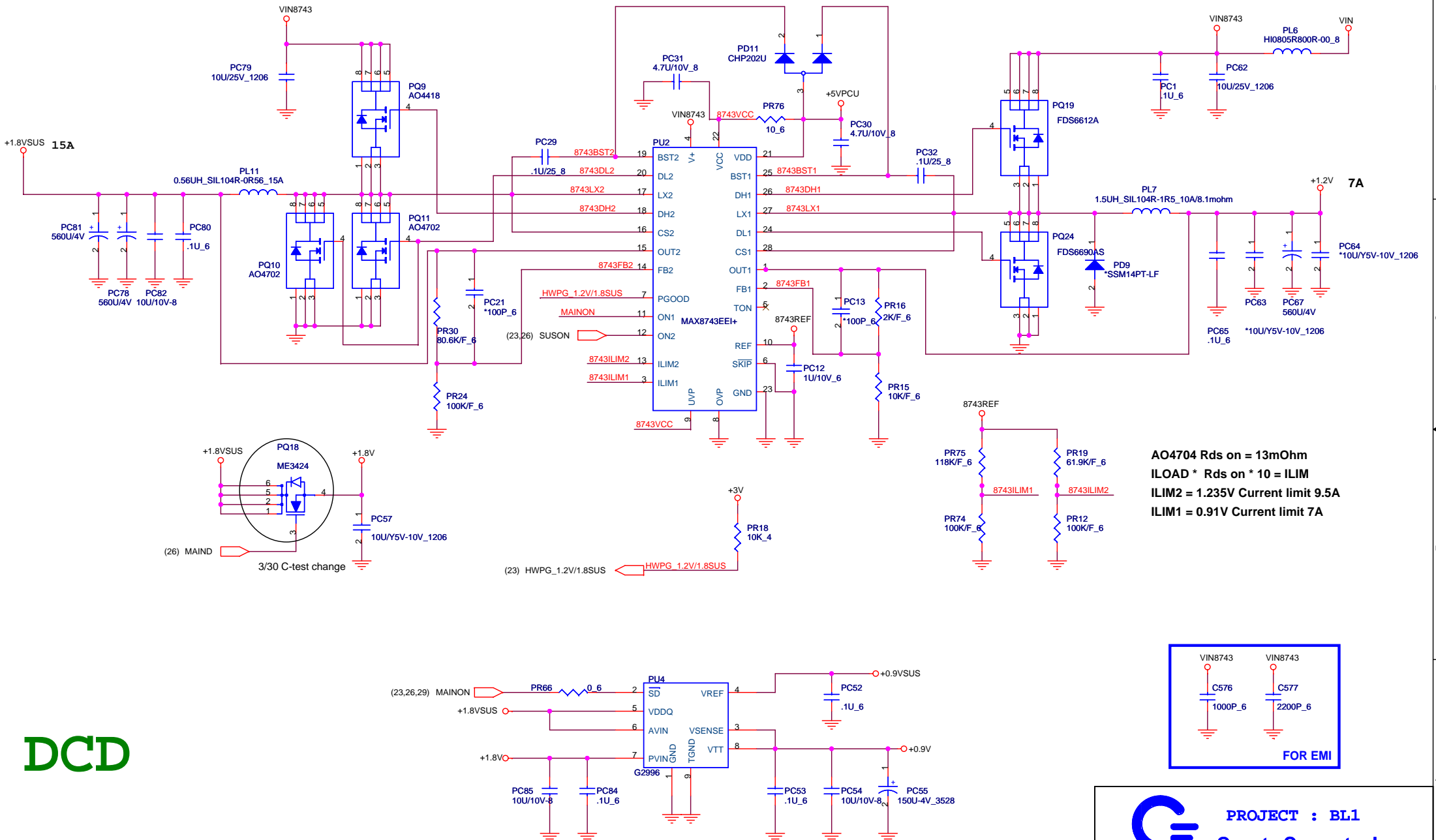
DCD



V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0		V
0	1	0	1	1	1	1	1.340
0	1	1	0	0	0	0	1.324
0	1	1	0	1	0	0	1.292
0	1	1	1	0	0	0	1.260
0	1	1	1	1	0	1	1.244
0	1	1	1	1	1	1	1.212
1	0	0	0	0	0	1	1.180
1	0	0	0	1	1	1	1.148
1	0	0	1	1	0	1	1.100
1	0	1	0	0	0	1	1.052
1	0	1	0	1	1	1	1.020
1	0	1	1	1	0	0	0.972
1	1	0	0	0	0	0	0.940

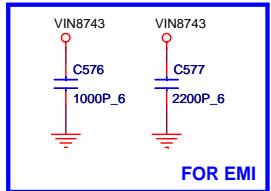






DCD

AO4704 Rds on = 13mOhm  
 ILOAD \* Rds on \* 10 = ILIM  
 ILIM2 = 1.235V Current limit 9.5A  
 ILIM1 = 0.91V Current limit 7A

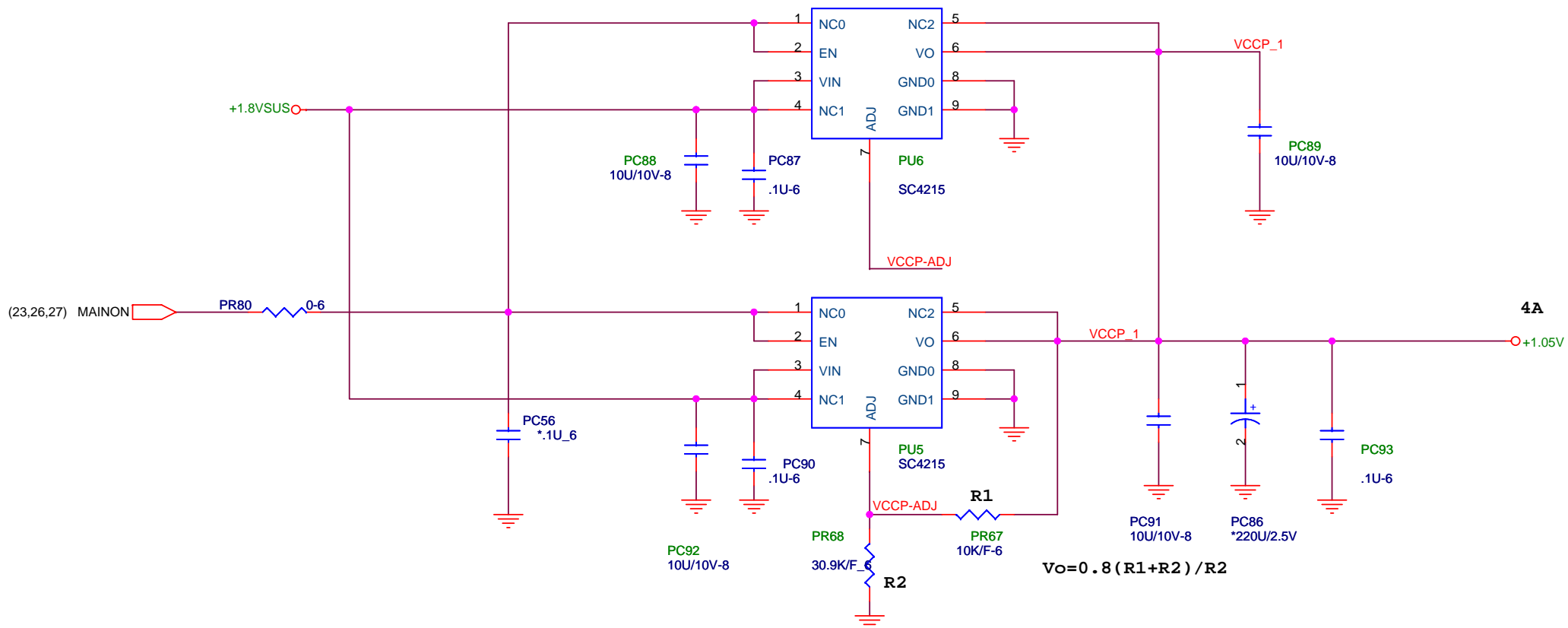


**PROJECT : BL1**

**Quanta Computer Inc.**

Size	Document Number <b>+1.8/1.2V / VTT</b>	Rev 1A
Date:	Friday, April 28, 2006	Sheet 27 of 30





PROJECT : BL1  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>+1.05V</b>	1A
Date:	Friday, April 28, 2006	Sheet 29 of 30